



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:

Constantin Bulucea and Rebecca Rossen

Assignee:

Siliconix incorporated

Title:

Trench DMOS Power Transistor With Field-Shaping Body Proffle and

Three-Dimensional Geometry

Application No.:

08/851,608

Filed:

5 May 1997

Examiner:

S. Crane

Group Art Unit:

2811

Docket No.:

M-799-4C US

San Jose, California 23 December 2002

BOX CPA COMMISSIONER FOR PATENTS Washington, D. C. 20231

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97(b)

Sir:

Pursuant to 37 CFR 1.56, 1.97, and 1.98, the documents listed on the accompanying substitute PTO Form 1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed, including translations where indicated. Copies of English abstracts of all the cited Japanese Patent Publications ("JPPs") are also enclosed, except for JPP 63-124762, a utility model JPP.

The present application is a file-wrapper continuation of parent U.S. patent application 08/453,285 which, in turn, is a file-wrapper continuation of grandparent U.S patent application 08/086,976. Hence all documents cited in parent application 08/453,285 and in grandparent application 08/086,976 are of record in the present application.

JPP 62-12167 was previously cited in grandparent application 08/086,976 and is re-cited here because an English translation of JPP 62-12167 is enclosed.

JPP 62-37965 was previously cited in grandparent application 08/086,976 using the partial number "0037965". JPP 62-37965 is re-cited here for clarity using its full publication

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Serial No.: 08/851/608

number. Also, the JPP 62-37965 publication date, previously given as 15 February 1987, is corrected here to 18 February 1987.

Blanchard, "Optimization of High Power MOS Transistors", was cited in parent application 08/453,285 and is re-cited here to identify the page numbers and indicate that the document is a Ph.D. dissertation.

Katoh et al, "Design of New Structural High Breakdown Voltage V-MOSFET -- Static Shield V-MOSFET", was cited earlier in this application and is re-cited here because a copy of the Japanese version of the document is enclosed.

Ueda et al, "High Speed Power MOSFET, U-MOS Power FET", was cited earlier in this application using the partial title "U-MOS Power FET" and is re-cited here (a) to present the full title and (b) because an English translation is enclosed. Inasmuch as the Japanese version of Ueda et al, "High Speed Power MOSFET, U-MOS Power FET", has two sets of page numbers, both sets of page numbers "335 - 442" and "143 - 150" are included here in the citation rather than the single set of page numbers "143 - 150" previously used in the citation.

Applicants' attorney does not have an English translation of Kato et al, "A Study for High Voltage V-MOS Structure". However, Kato et al, "A Study for High Voltage V-MOS Structure", appears to deal with material similar to that in Katoh et al, "Design of New Structural High Breakdown Voltage V-MOSFET—Static Shield V-MOSFET", and similar to that in Katoh et al, "Design of High Breakdown V-MOSFET Applying Static Shield Effect".

Applicants' attorney recognizes that the enclosed copies of some of the cited documents repeat copies previously provided to the PTO in connection with the present application, with parent application 08/453,285, or with grandparent application 08/086,976. To the extent that such accumulation of multiple copies may be inconsistent with PTO policy or rules, Applicants' attorney requests the Examiner to discard the earlier-provided copies.

Further enclosed to simplify printing of the present application is a Summary of all the Documents Cited, i.e., now of record, in the present application and suitable for being listed on the first page of the patent as "References Cited". In the enclosed Summary of Cited Documents, the citations for some of the journal articles have been simplified by deleting unnecessary material such as the names of authors after the first-named authors.

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Siliconix inc. ("Siliconix"), the assignee of the present application, is also the assignee of (a) U.S. Patent 5,072,266, the great grandparent of the present application, and (b) U.S. Patent 5,298,442, the great grandparent of the present application.

Siliconix sued Fairchild Semiconductor Corp. ("Fairchild") for infringement of U.S. Patents 5,072,266 and 5,298,442. The patent infringement suit, now settled, was brought in the Northern District of California as case no. 99-04797 SBA. In the infringement suit, Fairchild submitted a 66-page Response Chart in which Fairchild alleged that certain claims of U.S. Patents 5,072,266 and 5,298,442 were invalid as anticipated by, or/and obvious in view of, certain references cited in the Response Chart.

A copy of the Response Chart, dated 30 August 2000, is enclosed. Subject to the comments in the next two paragraphs, all of the documents cited in the Response Chart are included with the enclosed substitute PTO Form 1449 or are already of record in the present application including parent application 08/753,285 and grandparent application 08/086,976. Likewise, aside from the documents already of record in the present application, copies of all the documents cited in the Response Chart are included with the enclosed copies of the references cited in the substitute PTO Form 1449.

On page 3 of the Response Chart, the citation to Kato et al, "A Study of High Voltage V-MOS Structure", should apparently be Kato et al, "A Study for High Voltage V-MOS Structure". That is, "of" in the title should apparently be "for".

Page 3 of the Response Chart cites (a) Katoh et al, "Design of High Breakdown Voltage V-MOSFET Applying Static Shield Effect," IEICE Transactions C, Vol. 66, No. 6, 1983, and then (b) Kato et al, "High Voltage-ization Using Static Shield Effect", Electrical Communications Laboratories Technical Journal, Vol. 33, No. 2, 1984. As far as applicants' attorney can determine, these two documents are respective English and Japanese versions of a single reference. Also, the journal/date citation information appears to be wrong for the English version, item (a). Referring to the enclosed substitute PTO Form 1449 and the accompanying copies of the cited documents, items (a) and (b) appear to be Katoh et al, "Design of High Breakdown Voltage V-MOSFET Applying Static Shield Effect", Review of the Electrical Communications Laboratories (which is probably an alternative English translation of the Japanese journal translated into English as Electrical Communications

Laboratories Technical Journal for item b) while the remaining citation information is Vol.

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32, No. 6, 1984, pages 1107-1114, for the English version, and Vol. 33, No. 2, 1984, pages 257-268, for the Japanese version.

In the Siliconix/Fairchild patent infringement suit, Fairchild also submitted an Amended Initial Disclosure of Defendant Fairchild Semiconductor - Prior Art in which Fairchild cited over five hundred references, including references cited in the Response Chart. A copy of this Amended Initial Prior Art Disclosure, likewise dated 30 August 2000, is enclosed.

Certain of the references cited in the Amended Initial Prior Art Disclosure are classified as "102" or/and "103" references with respect to U.S. Patents 5,072,266 and 5,298,442. However, the Amended Initial Prior Art Disclosure does not cite any particular claim(s) of U.S. Patents 5,072,266 and 5,298,442, and does not provide any analogies between any of the claims of U.S. Patents 5,072,266 and 5,298,442, on one hand, and the material of any of the cited references, including the "102", "102/103", and "103" references, on the other hand. All of the "102" references, including three "102" references not mentioned in the Response Chart, are listed on the accompanying substitute PTO Form 1449 or are already of record in the present application.

Aside from the references cited in both the enclosed substitute PTO Form 1449 and the Amended Initial Prior Art Disclosure, Applicants' attorney has not obtained copies of and/or reviewed any of the further references cited in the Amended Initial Prior Art Disclosure in connection with the present application, and expresses no view as to the materiality of any of these further references to any of the claims of this application. The enclosed copy of the Amended Initial Prior Art Disclosure is provided in fulfillment of applicants' attorneys' obligation of candor and good faith with the PTO.

If the Response Chart and the Amended Initial Prior Art Disclosure themselves need to be listed on a (substitute) PTO Form 1449 in order for the Examiner to be obligated to consider these two Fairchild documents, please so inform Applicants' attorney.

Citation of the above documents shall not be construed as:

- 1. an admission that the documents are necessarily prior art with respect to the instant invention;
- 2. a representation that a search has been made; or

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3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 CFR 1.56(b).

Please telephone Applicants' attorney at 408-453-9200, ext. 1371, if there are any questions regarding this submission.

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Respectfully submitted,

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FAIRCHILD SEMICONDUCTOR

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

(OAKLAND DIVISION)

CASE NO. 99-04797 SBA

RESPONSE CHART

(Civil L.R. 16-9(b))

Pursuant to Civil Local Rule 16-9(b), Fairchild Semiconductor Corporation ("Fairchild") herein serves its response chart on Plaintiff Siliconix Incorporated Siliconix"). Fairchild provides the following claim invalidity analysis under 35 U.S.C. §§ 102 and 103.

I. INTRODUCTION

Local Rule 16-9(a) requires that the party alleging infringement of a patent must submit a claim chart which "must contain" information identifying "where each element of each infringed claim is found within each apparatus, product [or] device . . .". L.R. 16-9(a)(4). Siliconix's claim chart alleges that Claim 1 of U.S. Patent No. 5,072,266 ("the '266 patent") and Claims 17, 18, 19, 20, 22, 23 and 24 of U.S. Patent No. 5,298,442 ("the '442 patent") are infringed by the Fairchild FDS 6680A product. Siliconix has failed to provide a claim chart which applies the asserted claims of the '266 patent and '442 patent against any other Fairchild product. RESPONSE CHART PURSUANT TO CIVIL L.R. 16-9(b) DOCSSV2:500277.1 (Case No. C-99-04797 SBA)

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Accordingly, Siliconix should be precluded from asserting infringement of the '266 patent and/or '422 patent against any other Fairchild product. II. **RESPONSIVE CHART**

The following chart indicates which claims of the patent are anticipated by which pieces of prior art. Please note that the information in this document is provisional and subject to revision, for the following reasons:

- (i) Fairchild's position on the invalidity of particular claims will depend on how those claims are construed by the Court. Because claim construction has not yet occurred, Fairchild cannot take a final position on the bases for invalidity of disputed claims because the Court may construe those claims to mean something different from what Fairchild presently assumes them to mean.
 - (ii) Fairchild has not yet completed its search for prior art.
- (iii) Fairchild has not completed its discovery from Plaintiff. Depositions of the persons involved in the drafting and prosecution of the patent-in-suit, and of the inventor, for instance, will likely reveal information that affects the conclusions herein.

Fairchild reserves the right to revise and/or supplement the claim chart. Fairchild incorporates herein the prosecution file history of the '266 patent and the '442 patent.

Presently, Fairchild intends to rely upon the following prior art patents and references:

JP 55146976

JP 58137254

JP 62-16572 -

Physics and Technology of Power MOSFETs, Shi-Chung Sun, UMI Dissertation Services.

February 1982

Optimization of Discrete High Power MOS Transistors, Richard A. Blanchard, UMI

Dissertation Services, Dec. 1981

JP 62012167

U.S. Patent 4,420,379

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1	JP 63-124762	
2	JP 63-224260	
3	JP 59-181668	
4	JP 54-57871	
5	JP 57-72365	
6	JP 59-193064	
7	JP 60-28271	
8	JP_57-18365	
9	JP 59-80970	
10	U.S. Patent 4,345,265	
11	U.S. Patent 4,443,931	
12	U.S. Patent 4,532,534	
13	U.S. Patent 4,374,455	
14	U.S. Patent 4,767,722	
15	U.S. Patent 3,412,297	
16	U.S. Patent 4,783,694	
17	U.S. Patent 4,593,302	
18	Design of New Structural High Breakdown Voltage V-MOSFET – Static Shield V-	
19	MOSFET, Kuniharu Katoh and Yuki Shimada, Electronics and Communications in	
20	. Japan, Vol. 66-C, No. 6, 1983	
21	A Study of High Voltage V-MOS Structure, Kunihara Kato, et al., IEICE Transactions C.,	
22	Vol. 81, No. 7(ED81-4), 1981.	
23	Design of High Breakdown Voltage V-MOSFET Applying Static Shield Effect, Kunihara	
24	Kato, et al., IEICE Transactions C, Vol. 66, No. 6, 1983.	
25	High Voltage-ization Using Static Shield Effect, Kunihara Kato, et al., Electrical	
26	Communications Laboratories Technical Journal, Vol. 33, No. 2, 1984.	
27	U-MOS Power MOSFET, Daisuke Ueda, et al., National Technical Report, Vol. 29, No. 2,	
28	Apr. 1983	

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RESPONSE CHART PURSUANT TO CIVIL L.R. 16-9(b) (Case No. C-99-04797 SBA)

The Following References (referred hereinafter as "KATOH") Will Be Analyzed Together:

Design of New Structural High Breakdown Voltage V-MOSFET - Static Shield V-MOSFET, Kuniharu Katoh and Yuki Shimada, Electronics and Communications in Japan, Vol. 66-C, No. 6, 1983

A Study of High Voltage V-MOS Structure, Kunihara Katoh, et al., IEICE Transactions C., Vol. 81, No. 7(ED81-4), 1981.

Design of High Breakdown Voltage V-MOSFET Applying Static Shield Effect, Kunihara Katoh, et al., IEICE Transactions C, Vol. 66, No. 6, 1983.

High Voltage-ization Using Static Shield Effect, Kunihara Katoh, et al., Electrical Communications Laboratories Technical Journal, Vol. 33, No. 2, 1984.

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266 U.S. Patent 5,072,266 JP 55146976 14 CLAIM 1 1. A trench DMOS transistor cell comprising: Double Diffusion Insulating Gate Field Effect Transistor 15 a substrate of semiconductor material of heavily doped N+ layer (101) first electrical conductivity type; 16 a first covering layer of semiconductor material of said N- layer (102) first electrical conductivity type lying on the substrate; 17 a second covering layer of semiconductor material of P layer (3) second electrical conductivity type lying on the first 18 covering layer; a third covering layer of semiconductor material of N+ layer (104) 19 heavily doped said first electrical conductivity type and having a top surface and partly lying over the second the P layer (3) has a heavily doped P+ region (103) 20 which extends upward through the N+ layer (104) and covering layer, wherein a portion of the second covering which extends downward (110-1 and 110-2) into the Nlayer is heavily doped and this portion extends both 21 layer (102) vertically upward and downward, an upward portion extending through the third covering layer to the top 22 surface of the third covering layer and a downward portion extending downward into the first covering 23 a trench having a bottom surface and side surfaces and trench (5) with a bottom surface and side surfaces which 24 extending vertically downward from the top surface of extend vertically downward from the top surface of the the third covering layer through the third covering layer N+ layer (104) through the N+ layer (104), the P layer 25 (3) and through a portion of the N- (102) layer, wherein and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of the bottom surface of the trench (5) lies above a lowest

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the trench lies above a lowest part of the downward

electrically conducting semiconductor material

portion of the second covering layer;

positioned within the trench;

part of the downward portion of the P+ region of the P

layer.

semiconductor material (107)

1	a layer of oxide positioned within the trench between the	oxide (106)
	electrically conducting semiconductor material and the	
2	bottom and side surfaces of the trench; and	
	three electrodes electrically coupled to the electrically	three electrodes electrically coupled to the semiconductor
3	conducting semiconductor material, to the third covering	material (107), to the N+ layer (104) and to the N+
	layer and to the substrate, respectively.	substrate (101).

_	U.S. Patent No. 5,298,442	JP 55146976
7	CLAIM 17	
8	17. A method for providing a transistor, said method comprising the steps of:	Double Diffusion Insulating Gate Field Effect Transistor
9	providing a first region of a first conductivity type;	N+ layer (101) and N- layer (102)
0	providing a second region of a second conductivity type over said first region;	P layer (3) formed by a first diffusion
1	providing a third region of said first conductivity type such that said first and third regions are separated by	N+ layer (104) formed by a second diffusion
2	said second region; providing a trench through said third and second regions; and	trench (5) with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer (104) through the N+ layer (104), the P layer
4	providing a gate in said trench;	(3) and through a portion of the N- (102) layer. Al gate electrode (107)
5	wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said	the P layer (3) has a heavily doped P+ region (103) which extends upward through the N+ layer (104) and which extends downward (110-1 and 110-2) through the
5	trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an	N- layer (102) deeper than the trench (5)
7	avalanche breakdown occurs away from a surface of said trench.	
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, [CLAIM 18	
)	18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion	the P layer (3) has a heavily doped P+ region (103) laterally spaced from the trench (5)
1	of said second region which portion is adjacent said trench.	
2	CLAIM 19 19. The method of claim 17 wherein said first region	N+ layer (101) under N- layer (102)
,	comprises a first portion and a second portion over said first portion, said second portion being lighter doped	
1	than said first portion.	
۱ ا	CLAIM 20 20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
	breakdown is a reach-through breakdown across said second portion.	across the N- layer (102)
5	CLAIM 22	
- 1	21. The method of claim 17 further comprising the step	oxide (106)

1	CLAIM 23	
2	23. A method for providing a transistor, said method comprising the steps of:	Double Diffusion Insulating Gate Field Effect Transistor
3	providing a first region of a first conductivity type; providing a second region of said first conductivity type	N+ layer (101)
-	over said first region, said second region being lighter	N- layer (102)
4	doped than said first region;	
5	providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (3) formed by a first diffusion
6	providing a fourth region of said first conductivity type over said third region;	N+ layer (104) formed by a second diffusion
. 7	providing a trench through said fourth region and third	trench (5) with a bottom surface and side surfaces which
8	regions; and	extend vertically downward from the top surface of the N+ layer (104) through the N+ layer (104), the P layer (3) and through a portion of the N- (102) layer.
9	providing a gate in said trench;	Al gate electrode (107)
10	wherein a deepest part of said third regions is laterally spaced from said trench;	P layer (3) is laterally spaced from said trench
11	wherein a distance between said deepest part of said third region and said first region is less than a depletion	the distance between the deepest part of the P layer (3) and the N+ layer (101) is less than a depletion width of a
12	width of a planar junction which has the same doping profile as does said junction between said second and	planar junction which has the same doping profile as does the junction between the N- layer (102) and the P
13	third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	layer (3) at the deepest part of the P layer (3) and which is reverse biased around its breakdown voltage
14	CLAIM 24	
17	24. The method of claim 23 wherein said deepest part of	the deepest part of the P layer (3) is heavier doped (P+
15	said third region is doped heavier than a part of said third region which part is adjacent said trench.	region(103)) than the part of the P layer (3) adjacent trench (5)

U.S. Patent 5,072,266	JP 58137254
CLAIM 1	
A trench DMOS transistor cell comprising:	Insulated Gate Semiconductor Device See Fig. 7
substrate of semiconductor material of heavily doped strate conductivity type;	N+ layer (1)
first covering layer of semiconductor material of said rst electrical conductivity type lying on the substrate;	N- layer (2)
second covering layer of semiconductor material of cond electrical conductivity type lying on the first overing layer;	P layer (13)

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1	a third covering layer of semiconductor material of	N+ layer (14);
	heavily doped said first electrical conductivity type and	1 71 (12) 1 11 1 17 1 (12)
2	having a top surface and partly lying over the second	the P layer (13) has a heavily doped P+ region (19)
İ	covering layer, wherein a portion of the second covering	portion which extends upward through the N+ layer (14)
3	layer is heavily doped and this portion extends both	and which extends downward into the N- layer (2)
	vertically upward and downward, an upward portion	
4	extending through the third covering layer to the top	
	surface of the third covering layer and a downward	
5	portion extending downward into the first covering	
-	layer;	
6	a trench having a bottom surface and side surfaces and	trench with a bottom surface and side surfaces which
١	extending vertically downward from the top surface of	extend vertically downward from the top surface of the
7	the third covering layer through the third covering layer	N+ layer (14) through the N+ layer (104), the P layer
′	and the second covering layer and through a portion of	(13) and through a portion of the N- (19) layer, wherein
8	the first covering layer, wherein the bottom surface of	the bottom surface of the trench lies above a lowest part
°	the trench lies above a lowest part of the downward	of the downward portion of the P+ region of the P layer.
9	•	
9	portion of the second covering layer;	gate semiconductor material (17)
	electrically conducting semiconductor material	gate semiconductor material (17)
10	positioned within the trench;	
	a layer of oxide positioned within the trench between the	oxide insulating film (16)
11	electrically conducting semiconductor material and the	
Į.	bottom and side surfaces of the trench; and	
12	three electrodes electrically coupled to the electrically	three electrodes electrically coupled to the gate
	conducting semiconductor material, to the third covering	semiconductor material (17), to the N+ layer (14) and to
13	layer and to the substrate, respectively.	the N+ substrate (1).
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U.S. Patent No. 5,298,442	JP 58137254
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of:	Insulated Gate Semiconductor Device See Fig. 7
providing a first region of a first conductivity type;	N+ layer (1) and N- layer (2)
providing a second region of a second conductivity type over said first region;	P layer (13) formed by a first diffusion
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (14) formed by a second diffusion
providing a trench through said third and second regions; and	trench with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer (14) through the N+ layer (14), the P layer (13) and through a portion of the N- (2) layer.
providing a gate in said trench;	gate semiconductor material (17)

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1	wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said	the P layer (13) has a heavily doped P+ region (19) which extends upward through the N+ layer (14) and
2	trench so that, if a predetermined voltage is applied to	which extends downward through the N- layer (2) deeper than the trench
3	said gate and to said third region and another predetermined voltage is applied to said first region, an	than the deficit
4	avalanche breakdown occurs away from a surface of said trench.	
	3333	
5	CV ATACLO	
6	CLAIM 18	
	18. The method of claim 17 wherein said portion P of	the P layer (13) has a heavily doped P+ region (19)
7	said second region is doped heavier than another portion of said second region which portion is adjacent said	which is laterally spaced from the trench
8	trench. CLAIM 19	
	19. The method of claim 17 wherein said first region	N+ layer (1) under N- layer (2)
, 9	comprises a first portion and a second portion over said	14 layer (1) under 14 layer (2)
	first portion, said second portion being lighter doped	_
10	than said first portion.	
11	CLAIM 20	
••	20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
12	breakdown is a reach-through breakdown across said	across the N- layer (2)
	second portion.	
13	CLAIM 22	
	21. The method of claim 17 further comprising the step	oxide insulating film (16)
14	of providing an insulator between said surface of said trench and said gate.	
15	CLAIM 23	
13	23. A method for providing a transistor, said method	Insulated Gate Semiconductor Device
16	comprising the steps of:	
	providing a first region of a first conductivity type;	N+ layer (1)
17	providing a second region of said first conductivity type	N- Layer (2)
	over said first region, said second region being lighter	
18	doped than said first region;	
19	providing a third region of a second conductivity type	P layer (13) formed by a first diffusion
19	over said second region, said second and third regions forming a junction;	
20	providing a fourth region of said first conductivity type	N+ layer (14) formed by a second diffusion
	over said third region;	14 layer (14) formed by a second diffusion
21	providing a trench through said fourth region and third	V trench which extends vertically downward from the
	regions; and	top surface of the N+ layer (14) through the N+ layer
22	~	(14), the P layer (13) and through a portion of the N- (2)
23		layer.
23	providing a gate in said trench;	gate electrode (17)
24	wherein a deepest part of said third regions is laterally spaced from said trench;	P layer (13) is laterally spaced from said V trench
25	wherein a distance between said deepest part of said	the distance between the deepest part of the P layer (13)
رے	third region and said first region is less than a depletion	and the N+ layer (1) is less than a depletion width of a
26	width of a planar junction which has the same doping	planar junction which has the same doping profile as
_	profile as does said junction between said second and third regions at said deepest part of said third region and	does the junction between the N- layer (2) and the P layer
27	which is reverse biased around its breakdown voltage.	(13) at the deepest part of the P layer (13) and which is reverse biased around its breakdown voltage
-	which is reverse clased around its oreakdown voltage.	reverse orased around its oreazinown voltage

1	CLAIM 24	
2	24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	the P layer (13) has a heavily doped P+ region (19) which is laterally spaced from the trench
3		

٠	U.S. Patent 5,072,266	
6	CLAIM 1	JP 6216572
7	1. A trench DMOS transistor cell comprising:	Vertical-type Semiconductor Device and Manufacturing Method Therefore
8		See figs. 1(a) and 1(b)
9	a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (1)
0	a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (2)
2	a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (4)
3	a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering	N+ layer (8) (p. 11 of translation: "Contracted by an n+stype semiconductor layer 8, the p-type semiconductor layer 4 (channel region) thus forms long and short portions underneath the n+-type semiconductor layer 8."
5	layer is heavily doped and this portion extends both vertically upward and downward, an upward portion	p. 11 of translation: "Forming p+-type semiconductor
i	extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering	layers 3 in cells by photolithography is used as another way of reducing the likelihood of the punch-through phenomenon occurring in conventional DSA MOS
, 	layer;	FETs."
		the P layer (4) has a heavily doped P+ region (3) portion which extends upward through the N+ layer (1) and which extends downward into the N layer (2)
	a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of	p. 12 of translation: "The vertical-type semiconductor device in accordance with the present invention is
	the third covering layer through the third covering layer and the second covering layer and through a portion of	characterized by comprising a semiconductor substrate of a first conduction type whose principal surface is
	the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward portion of the second covering layer;	provided with a groove; a semiconductor film or conductor film pattern formed through the agency of a first insulating film over the groove formed in the
		principal surface of the semiconductor substrate"
	,	As seen from Fig. 1(b), the P layer (4) has a heavily doped P+ region (3) portion which extends upward
	electrically conducting and	through the N+ layer (8) and which extends downward into the N layer (2)
	electrically conducting semiconductor material positioned within the trench;	source Al electrode 9 is formed on this insulating film
		p. 12 of translation: " a semiconductor film or conductor film pattern formed through the agency of a
- 11	·	first insulating film over the groove formed in the

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RESPONSE CHART PURSUANT TO CIVIL L.R. 16-9(b) (Case No. C-99-04797 SBA)

1	a layer of oxide positioned within the trench between the	first insulating film (5a)
	electrically conducting semiconductor material and the	
2	bottom and side surfaces of the trench; and	
	three electrodes electrically coupled to the electrically	Source Al electrode (9a).
3	conducting semiconductor material, to the third covering	, ,
	layer and to the substrate, respectively.	Gate Al electrode (9b).
4		·
i		Since the device is a vertical-type semiconductor device,
5		the N+ layer (1) must have a drain electrode.
5		Since the device is a vertical-type semiconductor device the N+ layer (1) must have a drain electrode.

INVALIDITY CLAIM CHART F U.S. Patent No. 5,298,442	
CLAIM 17	JP 62-16572
17. A method for providing a transistor, said method	Vertical-type Semiconductor Device and Manufacturing
comprising the steps of:	Method Therefore
11: 6	See figs. 1(a) and 1(b)
providing a first region of a first conductivity type;	N+ layer (1) and N layer (2).
providing a second region of a second conductivity typ over said first region;	
providing a third region of said first conductivity type	N+ layer (8) (p. 11 of translation: "Contracted by an n+-
such that said first and third regions are separated by said second region;	type semiconductor layer 8, the p-type semiconductor layer 4 (channel region) thus forms long and short
	portions underneath the n+-type semiconductor layer 8.")
providing a trench through said third and second	p. 12 of translation: "The vertical-type semiconductor
regions; and	device in accordance with the present invention is
	characterized by comprising a semiconductor substrate of
	a first conduction type whose principal surface is provided with a groove; "
providing a gate in said trench;	p. 12 of translation: "a semiconductor film or
•	conductor film pattern formed through the agency of a
	first insulating film over the groove formed in the
wherein a portion P of said second region, which portion	principal surface of the semiconductor substrate" the P layer (4) has a heavily doped P+ region (3) which
s spaced from said trench, extends deeper than said	extends upward through the N+ layer (8) and which
rench so that, if a predetermined voltage is applied to	extends downward through the N- layer (2) deeper than
said gate and to said third region and another	the groove
predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of	
aid trench.	
-	
CLAIM 18	
18. The method of claim 17 wherein said portion P of	the P layer (4) has a heavily doped P+ region (3) which is
said second region is doped heavier than another portion	spaced away from the groove
of said second region which portion is adjacent said trench.	
CLAIM 19	
19. The method of claim 17 wherein said first region	N+ layer (1) under N layer (2).
comprises a first portion and a second portion over said	2
first portion, said second portion being lighter doped	
than said first portion.	

1	CLAIM 20	
	20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
2	breakdown is a reach-through breakdown across said	across the N layer (2)
	second portion.	
3	CLAIM 22	
	21. The method of claim 17 further comprising the step	first insulating film (5a)
4	of providing an insulator between said surface of said	
	trench and said gate.	
5	CLAIM 23	
	23. A method for providing a transistor, said method	Vertical-type Semiconductor Device and Manufacturing
6	comprising the steps of:	Method Therefore
. 7		See figs. 1(a) and 1(b)
	providing a first region of a first conductivity type;	N+ layer (1)
8	providing a second region of said first conductivity type	N layer (2)
	over said first region, said second region being lighter	
9	doped than said first region;	
10	providing a third region of a second conductivity type	P layer (4)
10	over said second region, said second and third regions	
.,	forming a junction;	•
11	providing a fourth region of said first conductivity type	N+ layer (8) (p. 11 of translation: "Contracted by an n+-
12	over said third region;	type semiconductor layer 8, the p-type semiconductor
12	·	layer 4 (channel region) thus forms long and short
13		portions underneath the n+-type semiconductor layer 8.")
		p. 12 of translation: "The vertical-type semiconductor
14	providing a trench through said fourth region and third regions; and	device in accordance with the present invention is
	regions, and	characterized by comprising a semiconductor substrate of
15		a first conduction type whose principal surface is
	·	provided with a groove; a semiconductor film or
16		conductor film pattern formed through the agency of a
		first insulating film over the groove formed in the
17		principal surface of the semiconductor substrate"
		Assess Complete (A) de Pile es (A) 1 1 1
18		As seen from Fig. 1(b), the P layer (4) has a heavily
		doped P+ region (3) portion which extends upward through the N+ layer (8) and which extends downward
19		into the N layer (2)
	providing a gate in said trench;	p. 12 of translation: "The vertical-type semiconductor
20	providing a gate in said denoti,	device in accordance with the present invention is
		characterized by comprising a semiconductor substrate of
21		a first conduction type whose principal surface is
22		provided with a groove;"
22		
23	·	p. 12 of translation: " a semiconductor film or
2.5		conductor film pattern formed through the agency of a
24		first insulating film over the groove formed in the principal surface of the semiconductor substrate"
- "	wherein a deepest part of said third regions is laterally	P layer (4) is laterally spaced from said groove.
25	spaced from said trench;	1 Tayor (4) is faterally spaced from said groove.
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wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	the distance between the deepest part of the P layer (3) and the N+ layer (1) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N layer (2) and the P layer (4) at the deepest part of the P layer (4) and which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	the P layer (4) has a heavily doped P+ region (3) which is spaced away from the groove

U.S. Patent 5,072,266	Physics and Technology of Power MOSFETs
CLAIM 1	
1. A trench DMOS transistor cell comprising:	VDMOS – see Figs. 2.1, 2.21 and 3.21
a substrate of semiconductor material of heavily dop	ed N+ layer
first electrical conductivity type;	
a first covering layer of semiconductor material of sa	aid N- layer
first electrical conductivity type lying on the substrate	te;
a second covering layer of semiconductor material o	f P layer
second electrical conductivity type lying on the first	
covering layer;	
a third covering layer of semiconductor material of	N+ layer
heavily doped said first electrical conductivity type	and
having a top surface and partly lying over the second	As seen in Fig. 2.1, a portion of the P layer is neavily
covering layer, wherein a portion of the second covering	bring doped P+; the P+ region extends vertically upward
layer is heavily doped and this portion extends both	around the N+ layer and downward into the N- layer
vertically upward and downward, an upward portion	1
extending through the third covering layer to the top	
surface of the third covering layer and a downward	
portion extending downward into the first covering	
layer;	
a trench having a bottom surface and side surfaces a	nd trench with a bottom surface and side surfaces which
extending vertically downward from the top surface	of extend vertically downward from the top surface of the
the third covering layer through the third covering la	ayer N+ layer through the N+ layer, the P layer and unough
and the second covering layer and through a portion	of portion of the N- layer.
the first covering layer, wherein the bottom surface	of
the trench lies above a lowest part of the downward	
portion of the second covering layer;	
electrically conducting semiconductor material	semiconductor material
positioned within the trench;	
a layer of oxide positioned within the trench between	en the oxide between the trench and gate
electrically conducting semiconductor material and	the
bottom and side surfaces of the trench; and	
three electrodes electrically coupled to the electrical	three electrodes electrically coupled to the semiconduc
conducting semiconductor material, to the third cov	rering material, to the top N+ layer and to the N+ substrate.
layer and to the substrate, respectively.	

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	U.S. Patent No. 5,298,442	Physics and Technology of Power MOSFETs
	CLAIM 17	
	method for providing a transistor, said method rising the steps of:	VDMOS – see Figs. 2.1, 2.21 and 3.21
	ling a first region of a first conductivity type;	N+ layer substrate and N- layer
provid	ling a second region of a second conductivity type	P layer formed by a first diffusion
provid	aid first region; ling a third region of said first conductivity type	N+ layer formed by a second diffusion
said s	hat said first and third regions are separated by econd region;	
	ding a trench through said third and second as; and	trench with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer through the N+ layer, the P layer and through
		portion of the N- layer.
provid	ding a gate in said trench;	Al gate electrode
where	ein a portion P of said second region, which portion	the P layer has a heavily doped P+ region which extend
is spa	ced from said trench, extends deeper than said a so that, if a predetermined voltage is applied to	upward through the N+ layer and which extends downward through the N- layer deeper than the trench.
said g	ate and to said third region and another termined voltage is applied to said first region, an	
avala	nche breakdown occurs away from a surface of rench.	
<u></u>	CLAIM 18	
18. T	he method of claim 17 wherein said portion P of	the P layer has a heavily doped P+ region which is
said s	econd region is doped heavier than another portion d second region which portion is adjacent said	laterally spaced away from the trench
trenc		
-	CLAIM 19	N+ layer substrate under the N- layer
	he method of claim 17 wherein said first region orises a first portion and a second portion over said	14. layor substrate under the 14- layor
first	portion, said second portion being lighter doped	
	said first portion.	
	CLAIM 20	
break	he method of claim 19 wherein said avalanche down is a reach-through breakdown across said	avalanche breakdown is a reach-through breakdown across the N- layer
	od portion. CLAIM 22	
of pr	he method of claim 17 further comprising the step oviding an insulator between said surface of said	oxide between the trench and gate
	h and said gate. CLAIM 23	
	A method for providing a transistor, said method prising the steps of:	VDMOS – see Figs. 2.1, 2.21 and 3.21
prov	iding a first region of a first conductivity type; iding a second region of said first conductivity type	N+ layer N- Layer
H	Advant a content region of cold tirel committee in its increase.	

1	providing a third region of a second conductivity type over said second region, said second and third regions	P layer formed by a first diffusion
2	forming a junction;	
	providing a fourth region of said first conductivity type	N+ layer formed by a second diffusion
3	over said third region;	
	providing a trench through said fourth region and third	trench with a bottom surface and side surfaces which
4	regions; and	extend vertically downward from the top surface of the
		N+ layer through the N+ layer, the P layer and through a
5		portion of the N- layer.
	providing a gate in said trench;	Al gate electrode
6	wherein a deepest part of said third regions is laterally	P layer is laterally spaced from said trench
	spaced from said trench;	
7	wherein a distance between said deepest part of said	the distance between the deepest part of the P layer and
	third region and said first region is less than a depletion	the N+ layer is less than a depletion width of a planar
8	width of a planar junction which has the same doping	junction which has the same doping profile as does the
	profile as does said junction between said second and	junction between the N- layer and the P layer at the
9	third regions at said deepest part of said third region and	deepest part of the P layer and which is reverse biased
	which is reverse biased around its breakdown voltage.	around its breakdown voltage
10	CLAIM 24	
	24. The method of claim 23 wherein said deepest part of	the P layer has a heavily doped P+ region which is
11	said third region is doped heavier than a part of said	laterally spaced away from the trench
	third region which part is adjacent said trench.	
12		

15 16	U.S. Patent 5,072,266	Optimization of Discrete High Power MOS Transistors
	CLAIM 1	
17	1. A trench DMOS transistor cell comprising:	VMOS Structure – see Fig. 4.22
	a substrate of semiconductor material of heavily doped	N+ layer
18	first electrical conductivity type;	
	a first covering layer of semiconductor material of said	N- layer
19	first electrical conductivity type lying on the substrate;	
	a second covering layer of semiconductor material of	P layer
20	second electrical conductivity type lying on the first	
	covering layer;	
21	a third covering layer of semiconductor material of	N+ layer;
	heavily doped said first electrical conductivity type and	1 D1 1 - 1 - 1 - 1 - 1 - 1 D1 ion mortion which
22	having a top surface and partly lying over the second	the P layer has a heavily doped P+ region portion which extends upward through the N+ layer and which extends
22	covering layer, wherein a portion of the second covering	downward into the N layer.
23	layer is heavily doped and this portion extends both	downward into the 14 tayor.
24	vertically upward and downward, an upward portion	
24	extending through the third covering layer to the top	
25	surface of the third covering layer and a downward	÷
23	portion extending downward into the first covering	
26	layer;	trench with a bottom surface and side surfaces which
20	a trench having a bottom surface and side surfaces and	extend vertically downward from the top surface of the
27	extending vertically downward from the top surface of	N+ layer through the N+ layer, the P layer and through a
۷,	the third covering layer through the third covering layer	portion of the N- layer.
၁၀	and the second covering layer and through a portion of	r

1.

1	the first covering layer, wherein the bottom surface of	
	the trench lies above a lowest part of the downward	
2	portion of the second covering layer;	
	electrically conducting semiconductor material	semiconductor material
3	positioned within the trench;	
	a layer of oxide positioned within the trench between the	oxide between the trench and gate
4	electrically conducting semiconductor material and the	
	bottom and side surfaces of the trench; and	
5	three electrodes electrically coupled to the electrically	three electrodes electrically coupled to the semiconductor
	conducting semiconductor material, to the third covering	material, to the top N+ layer and to the N+ substrate.
6	layer and to the substrate, respectively.	

U.S. Patent No. 5,298,442	Optimization of Discrete High Power MOS Transistors
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of:	VMOS Structure – see Fig. 4.22
providing a first region of a first conductivity type;	N+ layer substrate and N- layer
providing a second region of a second conductivity type over said first region;	P layer formed by a first diffusion
providing a third region of said first conductivity type	N+ layer formed by a second diffusion
such that said first and third regions are separated by said second region;	
providing a trench through said third and second regions; and	trench with a bottom surface and side surfaces which extend vertically downward from the top surface of the N+ layer through the N+ layer, the P layer and through
	portion of the N- layer.
providing a gate in said trench; wherein a portion P of said second region, which portion	Al gate electrode the P layer has a heavily doped P+ region which extend
is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to	upward through the N+ layer and which extends downward through the N- layer deeper than the trench.
said gate and to said third region and another predetermined voltage is applied to said first region, an	
avalanche breakdown occurs away from a surface of said trench.	
,	·
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion	the P layer has a heavily doped P+ region which is laterally spaced away from the trench
of said second region which portion is adjacent said trench.	
CLAIM 19	1 4 27 1
19. The method of claim 17 wherein said first region	N+ layer substrate under the N- layer
comprises a first portion and a second portion over said first portion, said second portion being lighter doped	
than said first portion.	

1	CLAIM.20	
	20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
2	breakdown is a reach-through breakdown across said	across the N- layer.
	second portion.	
3	CLAIM 22	·
	21. The method of claim 17 further comprising the step	oxide between the trench and gate
4	of providing an insulator between said surface of said	
	trench and said gate.	
5	CLAIM 23	
_	23. A method for providing a transistor, said method	VMOS Structure – see Fig. 4.22
6	comprising the steps of:	
_	providing a first region of a first conductivity type;	N+ layer
7	providing a second region of said first conductivity type	N- Layer
	over said first region, said second region being lighter	·
8	doped than said first region;	
9	providing a third region of a second conductivity type	P layer formed by a first diffusion
,	over said second region, said second and third regions	
10	forming a junction;	
	providing a fourth region of said first conductivity type	N+ layer formed by a second diffusion
11	over said third region;	
·	providing a trench through said fourth region and third	trench with a bottom surface and side surfaces which
12	regions; and	extend vertically downward from the top surface of the
		N+ layer through the N+ layer, the P layer and through a portion of the N- layer.
13	providing a gate in said trench;	Al gate electrode
	wherein a deepest part of said third regions is laterally	P layer is laterally spaced from said trench
14	spaced from said trench;	r layer is laterally spaced from said deficit
	wherein a distance between said deepest part of said	the distance between the deepest part of the P layer and
15	third region and said first region is less than a depletion	the N+ layer is less than a depletion width of a planar
. 16	width of a planar junction which has the same doping	junction which has the same doping profile as does the
10	profile as does said junction between said second and	junction between the N- layer and the P layer at the
17	third regions at said deepest part of said third region and	deepest part of the P layer and which is reverse biased
*/	which is reverse biased around its breakdown voltage.	around its breakdown voltage
18	CLAIM 24	
	24. The method of claim 23 wherein said deepest part of	the P layer has a heavily doped P+ region which is
19	said third region is doped heavier than a part of said	laterally spaced away from the trench
	third region which part is adjacent said trench.	
20		

22	U.S. Patent 5,072,266	R U.S. PATENT NO. 5,072,266 JP 62012167
3	CLAIM 1	
4	1. A trench DMOS transistor cell comprising:	Manufacture of Vertical Type Semiconductor Device with Groove Section
.5		See fig. 1(f).
26 27	a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (11) (p. 5 of the translation: "a n+-type semiconductor substrate 11 with a high concentration of impurities is coated with an n-type semiconductor layer 12 having a lower concentration of impurities.")
.8	a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (12)
	DOCSSV2:500277.1	RESPONSE CHART PURSUANT TO CIVIL L.R. 16-9(b

1	a second covering layer of semiconductor material of	P layer (16)
	second electrical conductivity type lying on the first	
2	covering layer;	
	a third covering layer of semiconductor material of	N+ layer (17) lying partly over the P layer (16)
3	heavily doped said first electrical conductivity type and	
	having a top surface and partly lying over the second	P layer (16) extends vertically upward through the N+
4	covering layer, wherein a portion of the second covering	layer (17) to the top surface and downward into the N
	layer is heavily doped and this portion extends both	layer (12)
5	vertically upward and downward, an upward portion	
	extending through the third covering layer to the top	
6	surface of the third covering layer and a downward	,
	portion extending downward into the first covering	
7	layer;	
	a trench having a bottom surface and side surfaces and	p. 6 of translation: "The grooved portion 20 has smooth
8	extending vertically downward from the top surface of	outlines and does not have any sharp pointed sections."
	the third covering layer through the third covering layer	
9	and the second covering layer and through a portion of	As seen from fig. 1(f), the grooved portion (20) extends
	the first covering layer, wherein the bottom surface of	upward through the N+ layer (17) and which extends
10	the trench lies above a lowest part of the downward	downward into the P layer (16) and the N layer (12)
	portion of the second covering layer;	
11	electrically conducting semiconductor material	p. 6 of translation: " polycrystalline silicon film 22
	positioned within the trench;	constituting a gate electrode"
12	a layer of oxide positioned within the trench between the	gate oxide film (21)
	electrically conducting semiconductor material and the	
13	bottom and side surfaces of the trench; and	
	three electrodes electrically coupled to the electrically	three electrodes electrically coupled to the semiconductor
14	conducting semiconductor material, to the third covering	material (22), to the top N+ layer (17) and to the N+
	layer and to the substrate, respectively.	substrate (11).
15	,	·
	II	

U.S. Patent No. 5,298,442	JP 62012167
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of:	Manufacture of Vertical Type Semiconductor Device with Groove Section
	See fig. 1(f).
providing a first region of a first conductivity type;	N+ layer (11) and N layer (12).
providing a second region-of a second conductivity type over said first region;	P layer (16).
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	N+ layer (17) lying above the P layer (16).
providing a trench through said third and second regions; and	p. 6 of translation: "The grooved portion 20 has smooth outlines and does not have any sharp pointed sections."
	As seen from fig. 1(f), the grooved portion (20) extends upward through the N+ layer (17) and which extends downward into the P layer (16) and the N layer (12)
providing a gate in said trench;	gate oxide film (21)

1 2 3 4	wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.	the P layer (16) extends upward through the N+ layer (17) and which extends downward through the N layer (12) deeper than the grooved portion (20)
5		
6	CLAIM 18	
U	18. The method of claim 17 wherein said portion P of	N/A
7	said second region is doped heavier than another portion	
	of said second region which portion is adjacent said	
8	trench.	·
	CLAIM 19	
9	19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped	N+ substrate (11) under N layer (12)
ı	than said first portion.	·
1	CLAIM 20	
12	20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion.	avalanche breakdown is a reach-through breakdown across the N layer (12)
	CLAIM 22	
13	21. The method of claim 17 further comprising the step	gata avida (21)
14	of providing an insulator between said surface of said trench and said gate.	gate oxide (21)
5	CLAIM 23	
_	23. A method for providing a transistor, said method	Manufacture of Vertical Type Semiconductor Device
6	comprising the steps of:	with Groove Section
7		See fig. 1(f).
	providing a first region of a first conductivity type;	N+ layer (11)
8	providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;	N layer (12)
0	providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (16)
1	providing a fourth region of said first conductivity type over said third region;	N+ layer (17) lying above the P layer (16)
2	providing a trench through said fourth region and third	p. 6 of translation: "The grooved portion 20 has smooth
3	regions; and	outlines and does not have any sharp pointed sections."
4	·	As seen from fig. 1(f), the grooved portion (20) extends upward through the N+ layer (17) and which extends downward into the P layer (16) and the N layer (12)
5	providing a gate in said trench;	gate oxide film (21)
	wherein a deepest part of said third regions is laterally	P layer (16) is laterally spaced from said groove.

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wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping	the distance between the deepest part of the P layer (16) and the N+ layer (11) is less than a depletion width of a planar junction which has the same doping profile as
profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	does the junction between the N- layer (12) and the P layer (16) at the deepest part of the P layer (16) and which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench.	N/A

- U.S. Patent 5,072,266	U.S. Patent 4,420,379
CLAIM 1	·
1. A trench DMOS transistor cell comprising:	Method for the Formation of Polycrystalline Silicon
	Layers, and its Application in the Manufacture of a Self
	Aligned, Non Planar, MOS Transistor
·	
	See Figs. 3-19.
a substrate of semiconductor material of heavily doped	N+ layer (20)
first electrical conductivity type;	
a first covering layer of semiconductor material of said	N- layer (21)
first electrical conductivity type lying on the substrate;	
a second covering layer of semiconductor material of	P layer (22), (25) and (27)
second electrical conductivity type lying on the first	
covering layer;	
a third covering layer of semiconductor material of	N+ layer (26)
heavily doped said first electrical conductivity type and	
having a top surface and partly lying over the second	the P layer has a heavily doped P+ region (22) which
covering layer, wherein a portion of the second covering	extends upward through the N+ layer (26) and which
layer is heavily doped and this portion extends both	extends downward into the N- layer (21)
vertically upward and downward, an upward portion	C-1 4 les 22 26 57- 45 - 45 - 5 - 5 - 5 - 5 - 5 - 5 - 5 -
extending through the third covering layer to the top	Col. 4, lns. 23-26: "In the stage shown as FIG. 5, the device undergoes an oxidizing treatment which
surface of the third covering layer and a downward	simultaneously deepens the P+ type guard ring and
portion extending downward into the first covering	protects the peripheral part of the junction under a thick
layer;	oxide layer 23 (1 micron), called the field oxide."
a trench having a bottom surface and side surfaces and	trench (30) with a bottom surface and side surfaces whi
extending vertically downward from the top surface of	extend vertically downward from the top surface of the
the third covering layer through the third covering layer	N+ layer (26) through the N+ layer (26), the P layer (23)
and the second covering layer and through a portion of	and through a portion of the N- (21) layer, wherein the
the first covering layer, wherein the bottom surface of	bottom surface of the trench (30) lies above a lowest pa
the trench lies above a lowest part of the downward	of the downward portion of the P layer (22)
portion of the second covering layer;	
electrically conducting semiconductor material	semiconductor material (32)
positioned within the trench;	
a layer of oxide positioned within the trench between the	oxide (31)
electrically conducting semiconductor material and the	
bottom and side surfaces of the trench; and	
three electrodes electrically coupled to the electrically	gate semiconductor material (32), source electrode (33)
conducting semiconductor material, to the third covering	and drain at N+ substrate (20)
layer and to the substrate, respectively.	

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U.S. Patent No. 5,298,442	U.S. Patent No. 4,420,379
CLAIM 17	, , , , , , , , , , , , , , , , , , , ,
17. A method for providing a transistor, said method	Method for the Formation of Polycrystalline Silicon
comprising the steps of:	Layers, and its Application in the Manufacture of a Se
	Aligned, Non Planar, MOS Transistor
	See Figs. 3-19.
providing a first region of a first conductivity type;	N+ layer (20) and N- layer (21)
providing a second region of a second conductivity type over said first region;	P layer (22), (25) and (27)
providing a third region of said first conductivity type	N+ layer (26)
such that said first and third regions are separated by said second region;	
providing a trench through said third and second	trench (30) through the N+ layer (26), the P layer (25)
regions; and	and through a portion of the N- (21) layer
providing a gate in said trench;	gate semiconductor material (32)
wherein a portion P of said second region, which portion	a portion of the P layer (22), which portion is spaced
is spaced from said trench, extends deeper than said	from the trench (30), extends deeper than the trench (3
trench so that, if a predetermined voltage is applied to	a morrion of the D.L. (22)
said gate and to said third region and another	a portion of the P Layer (22) acts as a guard rail to spre
predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of	the electric field at the periphery and away from the
said trench.	· ·
CLAIM 18	-
18. The method of claim 17 wherein said portion P of	P layer has a heavily doped P+ portion (22) which is
said second region is doped heavier than another portion	laterally spaced from the trench
of said second region which portion is adjacent said	
trench.	
CLAIM 19	
19. The method of claim 17 wherein said first region	N+ layer (20) under N- layer (21)
comprises a first portion and a second portion over said	· · · · · · · · · · · · · · · · · · ·
first portion, said second portion being lighter doped	
than said first portion.	
CLAIM 20	
20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said	avalanche breakdown is a reach-through breakdown
second portion.	across the N- layer (21)
CLAIM 22	
21. The method of claim 17 further comprising the step	oxide (31)
of providing an insulator between said surface of said	Oxide (31)
rench and said gate.	
CLAIM 23	
23. A method for providing a transistor, said method	Method for the Formation of Polycrystalline Silicon
comprising the steps of:	Layers, and its Application in the Manufacture of a Self
	Aligned, Non Planar, MOS Transistor
	See Figs. 3-19.

1	providing a second region of said first conductivity type over said first region, said second region being lighter	N- layer (21)
2	doped than said first region;	P1 (00) (05) 1 (05)
3	providing a third region of a second conductivity type over said second region, said second and third regions forming a junction;	P layer (22), (25) and (27)
4	providing a fourth region of said first conductivity type over said third region;	N+ layer (26)
5	providing a trench through said fourth region and third regions; and	trench (30) through the N+ layer (26) and the P layer (25) and through a portion of the N- (21) layer
6	providing a gate in said trench;	gate semiconductor material (32)
7	wherein a deepest part of said third regions is laterally spaced from said trench;	the P layer region (22) is laterally spaced from trench (30)
8	wherein a distance between said deepest part of said third region and said first region is less than a depletion	the distance between the deepest part of the P layer (22) and the N+ layer (20) is less than a depletion width of a
9	width of a planar junction which has the same doping profile as does said junction between said second and	planar junction which has the same doping profile as does the junction between the N- layer (21) and the P
10	third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	layer (22) at the deepest part of the P layer (22) and which is reverse biased around its breakdown voltage
11	CLAIM 24	
11	24. The method of claim 23 wherein said deepest part of	the deepest part of the third region is P+ and is doped
12	said third region is doped heavier than a part of said third region which part is adjacent said trench.	heavier than the part of the third region P (25) adjacent the trench

U.S. Patent 5,072,266	JP 63-124762
CLAIM 1	
1. A trench DMOS transistor cell comprising:	Vertical MOSFET
	See fig. 1
a substrate of semiconductor material of heavily doped	N+ layer (1)
first electrical conductivity type;	
a first covering layer of semiconductor material of said	N layer (2)
first electrical conductivity type lying on the substrate;	
a second covering layer of semiconductor material of	P layer (3), (11) and (12)
second electrical conductivity type lying on the first	
covering layer;	
a third covering layer of semiconductor material of	N+ layer (4) lying partly over the P layer (3)
heavily doped said first electrical conductivity type and	A - and an a Caller D lawer (11) and (12) in heavile down t
having a top surface and partly lying over the second	A portion of the P layer (11) and (12) is heavily doped P+ and extends upward through the N+ layer (4) to the
covering layer, wherein a portion of the second covering	top and downward into the N layer (2).
layer is heavily doped and this portion extends both vertically upward and downward, an upward portion	top and downward into the 14 layer (2).
extending through the third covering layer to the top	
surface of the third covering layer and a downward	
portion extending downward into the first covering	
layer;	
a trench having a bottom surface and side surfaces and	trench (8) having a bottom surface and side surfaces an
extending vertically downward from the top surface of	extending vertically downward from the top surface of
the third covering layer through the third covering layer	the N+ layer (4) through the N+ layer (4) and the P layer

1	and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of	(3) and through a portion of the N layer (2), wherein the bottom surface of the trench (8) lies above a lowest part
2	the trench lies above a lowest part of the downward	of the P+ layer (12)
	portion of the second covering layer;	
3	electrically conducting semiconductor material	trench (8) possess a highly doped poly-silicon gate
	positioned within the trench;	electrode (9)
4	a layer of oxide positioned within the trench between the	gate oxide film (7)
	electrically conducting semiconductor material and the	
5	bottom and side surfaces of the trench; and	
	three electrodes electrically coupled to the electrically	gate electrode (9), source electrode (14) and drain
6	conducting semiconductor material, to the third covering	electrode (15)
	layer and to the substrate, respectively.	

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442		
U.S. Patent No. 5,298,442	JP 63-124762	
CLAIM 17		
17. A method for providing a transistor, said method	Vertical MOSFET	
comprising the steps of :		
Comprising the steps of the	See fig. 1	
providing a first region of a first conductivity type;	N+ layer (1) and N layer (2)	
providing a second region of a second conductivity type	P layer (3), (11) and (12)	
over said first region;		
providing a third region of said first conductivity type	N+ layer (4) such that P layer (3) is between the N layer	
such that said first and third regions are separated by	(2) and the N+ layer (4)	
said second region;		
providing a trench through said third and second	trench (8) extending through the N+ layer (4) and the F	
regions; and	layer (3)	
providing a gate in said trench;	trench (8) possess a highly doped poly-silicon gate	
	portion P+ (12) is spaced from trench (8) and extends	
wherein a portion P of said second region, which portion	deeper than said trench (8) so that, if a predetermined	
is spaced from said trench, extends deeper than said	voltage is applied to the gate (9) and to N+ layer (4) an	
trench so that, if a predetermined voltage is applied to	another predetermined voltage is applied to the N+ layer	
said gate and to said third region and another predetermined voltage is applied to said first region, an	(1), an avalanche breakdown occurs away from a surfa	
avalanche breakdown occurs away from a surface of	of the trench (8).	
said trench.	·	
Salu uchen.		
CLAIM 18		
18. The method of claim 17 wherein said portion P of	A portion of the P layer (11) and (12) is heavily doped	
said second region is doped heavier than another portion	P+	
of said second region which portion is adjacent said		
trench.	P layer (3) is adjacent the trench (8)	
CLAIM 19		
19. The method of claim 17 wherein said first region	N+ layer (1) under N layer (2)	
comprises a first portion and a second portion over said		
first portion, said second portion being lighter doped	•	
than said first portion.		

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1 [CLAIM 20	
	20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
2	breakdown is a reach-through breakdown across said	across the N layer (2)
	second portion.	
3	CLAIM 22	
	21. The method of claim 17 further comprising the step	gate oxide film (7)
4	of providing an insulator between said surface of said	,
	trench and said gate.	
5	CLAIM 23	
Ì	23. A method for providing a transistor, said method	Vertical MOSFET
6	comprising the steps of:	
	•	See fig. 1
7	providing a first region of a first conductivity type;	N+ layer (1)
	providing a second region of said first conductivity type	N layer (2)
8	over said first region, said second region being lighter	
	doped than said first region;	
9	providing a third region of a second conductivity type	P layer (3), (11) and (12) over N layer (2)
	over said second region, said second and third regions	
10	forming a junction;	
11	providing a fourth region of said first conductivity type	N+ layer (4) lying above the P layer (3).
11	over said third region;	
12	providing a trench through said fourth region and third	trench (8) through N+ layer (4) and P layer (3)
12	regions; and	
13	providing a gate in said trench;	gate oxide film (9)
15	wherein a deepest part of said third regions is laterally	portions of P layer (11) and (12) are laterally spaced from
14	spaced from said trench;	trench (8)
	wherein a distance between said deepest part of said	the distance between the deepest part of the P layer (12)
15	third region and said first region is less than a depletion	and the N+ layer (1) is less than a depletion width of a
	width of a planar junction which has the same doping	planar junction which has the same doping profile as
16	profile as does said junction between said second and	does the junction between the N- layer (2) and the P layer (12) at the deepest part of the P layer (12) and which is
	third regions at said deepest part of said third region and	reverse biased around its breakdown voltage
17	which is reverse biased around its breakdown voltage.	reverse diased around its dieakdown voltage
	CLAIM 24	to the standard major in D (12) and in
18	24. The method of claim 23 wherein said deepest part of	the deepest part of the third region is P+ (12) and is doped heavier than the part of the third region P (3)
	said third region is doped heavier than a part of said	
19	third region which part is adjacent said trench.	adjacent the trench (8)
	П	

21 **INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266** JP 63-224260 U.S. Patent 5,072,266 22 CLAIM 1 23 1. A trench DMOS transistor cell comprising: VMOS FET 24 See fig. 1 P layer (11) (opposite conductivity type with respect to a substrate of semiconductor material of heavily doped 25 drain). first electrical conductivity type; N- layer (12) a first covering layer of semiconductor material of said 26 first electrical conductivity type lying on the substrate; P layer (13) (20) lying on N layer (12) a second covering layer of semiconductor material of 27 second electrical conductivity type lying on the first

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covering layer;

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- 1		
1	a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and	N+ layer (14) lying partly over the P layer (13), wherein a portion of the P layer (20) is heavily doped P+ and
2	having a top surface and partly lying over the second covering layer, wherein a portion of the second covering	extends downward into the N- Layer (12)
3	layer is heavily doped and this portion extends both vertically upward and downward, an upward portion	
4	extending through the third covering layer to the top	
5	surface of the third covering layer and a downward portion extending downward into the first covering	
	layer;	
6	a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of	trench (15) having a bottom surface and side surfaces and extends vertically downward from the top surface of N+
7	the third covering layer through the third covering layer and the second covering layer and through a portion of	layer (14) through the N+ layer (14) and the P layer (13) and through a portion of the N- layer (12), wherein the
8	the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward	bottom surface of the trench (15) lies above the lowest part of the downward portion of the P layer (20) which is heavily doped
9	portion of the second covering layer;	
	electrically conducting semiconductor material	poly gate material (18) in trench (15)
10	positioned within the trench;	
	a layer of oxide positioned within the trench between the	gate oxide film (17)
11	electrically conducting semiconductor material and the	
	bottom and side surfaces of the trench; and	
12	three electrodes electrically coupled to the electrically	gate electrode (18), source electrode (9) and drain
	conducting semiconductor material, to the third covering	electrode (24)
13	layer and to the substrate, respectively.	

i	INVALIDITY CLAIM CHART FOR	
16	U.S. Patent No. 5,298,442	JP 63-224260
_	CLAIM 17	
7 1	7. A method for providing a transistor, said method	VMOS FET
18 C	comprising the steps of:	
	·	See fig. 1
ع وا	providing a first region of a first conductivity type;	N- layer (12).
	providing a second region of a second conductivity type	P layer (16) and (20)
	over said first region;	1 21 (10)
l p	providing a third region of said first conductivity type	N+ layer (14) lying above the P layer (16)
	such that said first and third regions are separated by	
s	said second region;	1 (17) and Player
22 F	providing a trench through said third and second	trench (15) extends through N+ layer (17) and P layer
1	regions; and	(16)
23 L	providing a gate in said trench;	poly gate (18)
	wherein a portion P of said second region, which portion	a portion of the P layer (20) is laterally spaced from the
24 i	is spaced from said trench, extends deeper than said	trench (15) and extends deeper than the trench (15)
t	trench so that, if a predetermined voltage is applied to	·
25	said gate and to said third region and another	
1	predetermined voltage is applied to said first region, an	
- V 11	avalanche breakdown occurs away from a surface of	
] :	said trench.	×
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SILICON VALLEY

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1	CLAIM 18	
1	18. The method of claim 17 wherein said portion P of	a portion P of the P layer is P+ (20) and is doped heavier
2	said second region is doped heavier than another portion	than the portion (26) of the P layer adjacent the trench
	of said second region which portion is adjacent said	(15)
3	trench.	
ſ	CLAIM 19	
4	19. The method of claim 17 wherein said first region	N/A
	comprises a first portion and a second portion over said	
5	first portion, said second portion being lighter doped	
	than said first portion.	
6	CLAIM 20	
	20. The method of claim 19 wherein said avalanche	N/A
7	breakdown is a reach-through breakdown across said	
	second portion.	
8 [CLAIM 22	
	21. The method of claim 17 further comprising the step	gate oxide film (17)
9	of providing an insulator between said surface of said	
10	trench and said gate.	
10	CLAIM 23	10.000
11	23. A method for providing a transistor, said method	VMOS FET
	comprising the steps of:	C 5- 1
12		See fig. 1. P substrate (11)
ŀ	providing a first region of a first conductivity type;	N layer (12)
13	providing a second region of said first conductivity type	N layer (12)
	over said first region, said second region being lighter doped than said first region;	
14	providing a third region of a second conductivity type	P layer (13) and (20)
_	over said second region, said second and third regions	- 1.5/01 (1.5/) === (==)
15	forming a junction;	
.	providing a fourth region of said first conductivity type	N+ layer (14) lying above P layer (13)
16	over said third region;	
17	providing a trench through said fourth region and third	trench (15) extending through N+ layer (13) and P layer
1/	regions; and	(13)
18	providing a gate in said trench;	poly gate (18)
-	wherein a deepest part of said third regions is laterally	the deepest part of the P layer (20) is laterally spaced
19	spaced from said trench;	from trench (15)
	wherein a distance between said deepest part of said	the distance between the deepest part of the P layer (20)
20	third region and said first region is less than a depletion	and the P layer (11) is less than a depletion width of a
	width of a planar junction which has the same doping	planar junction which has the same doping profile as
21	profile as does said junction between said second and	does the junction between the N- layer (12) and the P
	third regions at said deepest part of said third region and	layer (20) at the deepest part of the P layer (20) and
22	which is reverse biased around its breakdown voltage.	which is reverse biased around its breakdown voltage
	CLAIM 24	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
23	24. The method of claim 23 wherein said deepest part of	the deepest part of the third region is P+ (20) which is doped heavier than the part of the third region adjacent
24	said third region is doped heavier than a part of said	the trench (15)
24	third region which part is adjacent said trench.	The deficit (13)
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SILICON VALLEY

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1	INVALIDITY CLAIM CHART FO	R U.S. PATENT NO. 5,072,266
2	U.S. Patent 5,072,266	JP 59-181668
	CLAIM 1	
3	1. A trench DMOS transistor cell comprising:	VMOS FET
4		See fig. 3
5	a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (11) and (12)
6	a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (13)
7	a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (14) and (16) lying on N layer (13)
8	a third covering layer of semiconductor material of	N+ layer (15) lying partly over the P layer (14), wherein
9	heavily doped said first electrical conductivity type and having a top surface and partly lying over the second	a portion of the P layer is a heavily doped P+ (16) and extends vertically upward through the N+ layer (15) and
10	covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both	vertically downward into the N layer (13)
11	vertically upward and downward, an upward portion extending through the third covering layer to the top	·
12	surface of the third covering layer and a downward portion extending downward into the first covering	
13	layer; a trench having a bottom surface and side surfaces and	trench (21) having a bottom surface and side surface and
14	extending vertically downward from the top surface of the third covering layer through the third covering layer	extending vertically downward through the N+ layer (15), the P layer (14) and through a portion of the N layer
15	and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of	(13), wherein the bottom surface of the trench (21) lies above the lowest part of the P layer (16).
16	the trench lies above a lowest part of the downward portion of the second covering layer;	
17	electrically conducting semiconductor material positioned within the trench;	poly gate in trench (19)
18	a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the	gate oxide layer (17)
19	bottom and side surfaces of the trench; and three electrically coupled to the electrically	gate electrode (19), source electrode (20) and drain
20	conducting semiconductor material, to the third covering layer and to the substrate, respectively.	electrode (not shown)

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U.S. Patent No. 5,298,442	JP 59-181668	
CLAIM 17		
17. A method for providing a transistor, said method	VMOS FET	
comprising the steps of:		
	See fig. 3	
providing a first region of a first conductivity type;	N+ layer (11) and (12), and N layer (13)	
providing a second region of a second conductivity type	P layer (14) and (16) lying on N layer (13)	
over said first region;		

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1	providing a third region of said first conductivity type	N+ layer (15) lying wherein N layer (13) and N+ layer
	such that said first and third regions are separated by	(15) are separated by P layer (14)
2	said second region;	
	providing a trench through said third and second	trench (21) extending vertically downward through the
3	regions; and	N+ layer (15) and P layer (14)
	providing a gate in said trench;	poly gate in trench (19)
4	wherein a portion P of said second region, which portion	a portion of the P layer (16), which is spaced from the
	is spaced from said trench, extends deeper than said	trench, extends deeper than the trench (21)
5	trench so that, if a predetermined voltage is applied to	
	said gate and to said third region and another	
6	predetermined voltage is applied to said first region, an	
7	avalanche breakdown occurs away from a surface of	
	said trench.	
8		
	CLAIM 18	
9	18. The method of claim 17 wherein said portion P of	a portion of the P layer (14) is a heavily doped P+ (16)
	said second region is doped heavier than another portion	which is laterally spaced from the trench (21)
10	of said second region which portion is adjacent said	
	trench.	
11	CLAIM 19	
12	19. The method of claim 17 wherein said first region	N+ layer (11) and (12) under N layer (13)
12	comprises a first portion and a second portion over said	
13	first portion, said second portion being lighter doped	
13	than said first portion.	
14	CLAIM 20	
17	20. The method of claim 19 wherein said avalanche	avalanched breakdown is a reach-through breakdown
15	breakdown is a reach-through breakdown across said	across the N layer (13)
••	second portion.	
16	CLAIM 22	
	21. The method of claim 17 further comprising the step	gate oxide layer (17)
17	of providing an insulator between said surface of said	
	trench and said gate.	
18	CLAIM 23	
	23. A method for providing a transistor, said method	VMOS FET
19	comprising the steps of:	
		See fig. 3
20	providing a first region of a first conductivity type;	N+ layer (11) and (12)
	providing a second region of said first conductivity type	N layer (13)
21	over said first region, said second region being lighter	
	doped than said first region;	
22	providing a third region of a second conductivity type	P layer (14) and (16) lying on N layer (13)
	over said second region, said second and third regions	·
23	forming a junction;	
	providing a fourth region of said first conductivity type	N+ layer (15) lying over the P layer (14)
24	over said third region;	·
25	providing a trench through said fourth region and third	trench (21) extending vertically downward through the
25	regions; and	N+ layer (15) and P layer (14)
26	providing a gate in said trench;	gate oxide layer (17)
26	wherein a deepest part of said third regions is laterally	a portion of the P layer (16) is laterally spaced from the
27	spaced from said trench;	trench (21)
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wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and	the distance between the deepest part of the P layer (16) and the N+ layer (12) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N layer (13) and the P layer (16) at the deepest part of the P layer (16) and
which is reverse biased around its breakdown voltage.	which is reverse biased around its breakdown voltage
CLAIM 24	
24. The method of claim 23 wherein said deepest part of	the deepest part of the third region is P+ region (16)
said third region is doped heavier than a part of said	which is doped heavier than P region (14) adjacent the
third region which part is adjacent said trench.	trench (21)

		:
8	INVALIDITY CLAIM CHART FO	R U.S. PATENT NO. 5.072.266
9	U.S. Patent 5,072,266	JP 54-57871
	CLAIM 1	
10	1. A trench DMOS transistor cell comprising:	VMOS FET
11	· .	See fig. 2
12	a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (1)
13	a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (2)
14	a second covering layer of semiconductor material of second electrical conductivity type lying on the first	P layer (3) and (10)
15	a third covering layer of semiconductor material of	N+ layer (4) lying partly over the P layer (3), wherein a
16	heavily doped said first electrical conductivity type and having a top surface and partly lying over the second	portion of the P layer is a heavily doped P+ (10) and extends vertically upward through the N+ layer (4) and
17	covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both	vertically downward into the N layer (2)
18	vertically upward and downward, an upward portion extending through the third covering layer to the top	
19	surface of the third covering layer and a downward portion extending downward into the first covering	
20	layer; a trench having a bottom surface and side surfaces and	trench (11) having a bottom surface and side surfaces and
21	extending vertically downward from the top surface of the third covering layer through the third covering layer	extending vertically downward through the N+ layer (4), the P layer (3) and through a portion of the N layer (2),
22	and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of	wherein the bottom surface of the trench (11) lies above the lowest part of the P layer (10)
23	the trench lies above a lowest part of the downward portion of the second covering layer;	
24	electrically conducting semiconductor material positioned within the trench;	Al gate (6) in trench (11)
25	a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the	gate oxide layer (5)
26	bottom and side surfaces of the trench; and	
27	three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering	gate electrode (6), source electrode (7) and drain electrode (9)

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layer and to the substrate, respectively.

U.S. Patent No. 5,298,442	JP 54-57871
CLAIM 17	
17. A method for providing a transistor, said method	VMOS FET
comprising the steps of:	
	See fig. 2
providing a first region of a first conductivity type;	N+ layer (1) and N layer (2).
providing a second region of a second conductivity type	P layer (3) and (10).
over said first region;	N. 1 (4) 1 1 1 1 1 1 1 (2)
providing a third region of said first conductivity type	N+ layer (4) lying above the P layer (3).
such that said first and third regions are separated by	
said second region;	the trench (11) extends through the N+ layer (4) and th
providing a trench through said third and second	P layer (3)
regions; and	Al gate (6) in trench (11)
providing a gate in said trench; wherein a portion P of said second region, which portion	the P layer (10) extends upward through the N+ layer
is spaced from said trench, extends deeper than said	(17) and which extends downward through the N- layer
trench so that, if a predetermined voltage is applied to	(12)
said gate and to said third region and another	
predetermined voltage is applied to said first region, an	
avalanche breakdown occurs away from a surface of	
said trench.	
CLAIM 18	
18. The method of claim 17 wherein said portion P of	a portion P of the second region (10) is doped heavier
said second region is doped heavier than another portion	than another portion (3) of the second region which is
of said second region which portion is adjacent said	adjacent the trench (11)
trench. CLAIM 19	
19. The method of claim 17 wherein said first region	N+ layer (1) under N layer (2)
comprises a first portion and a second portion over said	111 16/01 (1) 011001 11 16/01 (2)
first portion, said second portion being lighter doped	
than said first portion.	
CLAIM 20	
20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
breakdown is a reach-through breakdown across said	across N layer (2)
second portion.	
CLAIM 22	
21. The method of claim 17 further comprising the step	gate oxide layer (5)
of providing an insulator between said surface of said	
trench and said gate.	
CLAIM 23	La con TETT
23. A method for providing a transistor, said method	VMOS FET
comprising the steps of:	San fig. 2
	See fig. 2
providing a first region of a first conductivity type;	N+ layer (1)
providing a second region of said first conductivity type	N layer (2)
over said first region, said second region being lighter	
doped than said first region;	P layer (3) and (10)
providing a third region of a second conductivity type	1 layer (3) and (10)
over said second region, said second and third regions	
forming a junction;	

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1	providing a fourth region of said first conductivity type over said third region;	N+ layer (4) lying above the P layer (3)
2	providing a trench through said fourth region and third regions; and	trench (11) through N+layer (4) and P layer (3)
3	providing a gate in said trench;	gate oxide film (5)
4	wherein a deepest part of said third regions is laterally spaced from said trench;	P layer (10) is laterally spaced from trench (11)
5	wherein a distance between said deepest part of said third region and said first region is less than a depletion	the distance between the deepest part of the P layer (10) and the N+ layer (1) is less than a depletion width of a
6	width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and	planar junction which has the same doping profile as does the junction between the N layer (2) and the P layer
7	which is reverse biased around its breakdown voltage.	(10) at the deepest part of the P layer (10) and which is reverse biased around its breakdown voltage
ا ہ	CLAIM 24	
8	24. The method of claim 23 wherein said deepest part of	the deepest part of the third region (10) is doped heavier
	said third region is doped heavier than a part of said	than part (3) which is adjacent the trench (11)
9	third region which part is adjacent said trench.	

13	U.S. Patent 5,072,266	JP 57-72365
13	CLAIM 1	
14	1. A trench DMOS transistor cell comprising:	VMOS FET
15		See fig. 1
13	a substrate of semiconductor material of heavily doped	P+ substrate (1)
16	first electrical conductivity type;	
	a first covering layer of semiconductor material of said	N layer (2)
17	first electrical conductivity type lying on the substrate;	
	a second covering layer of semiconductor material of	P layer (3) and (4)
18	second electrical conductivity type lying on the first	
	covering layer;	
19	a third covering layer of semiconductor material of	N+ layer (5) lying partly over the P layer (4), wherein the
	heavily doped said first electrical conductivity type and	P layer is heavily doped P+ and extends both vertically
20	having a top surface and partly lying over the second	upward through the N+ layer (5) and downward into the
	covering layer, wherein a portion of the second covering	N layer (2)
21	layer is heavily doped and this portion extends both	
	vertically upward and downward, an upward portion	
22	extending through the third covering layer to the top	, i
	surface of the third covering layer and a downward	
23	portion extending downward into the first covering	
. 4	layer; a trench having a bottom surface and side surfaces and	trench (6) having a bottom surface and side surfaces and
24	extending vertically downward from the top surface of	extending vertically through the N+ layer (5) and the P
25	the third covering layer through the third covering layer	layer (4), and through a portion of the N layer (2), where
23	and the second covering layer and through a portion of	the bottom surface of the trench (6) lies above the lowest
26	the first covering layer, wherein the bottom surface of	part of the P layer (3)
.0	the trench lies above a lowest part of the downward	ļ ·
27	portion of the second covering layer;	
- /	electrically conducting semiconductor material	metal layer (8)
28	positioned within the trench;	
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1	a layer of oxide positioned within the trench between the	gate oxide (7)
	electrically conducting semiconductor material and the	
2	bottom and side surfaces of the trench; and	
	three electrodes electrically coupled to the electrically	gate electrode (8), source electrode (9) and drain (D)
3	conducting semiconductor material, to the third covering	
	layer and to the substrate, respectively.	

U.S. Patent No. 5,298,442	JP 57-72365
CLAIM 17	
17. A method for providing a transistor, said method	VMOS FET
comprising the steps of:	i '
	See fig. 1
providing a first region of a first conductivity type;	N layer (2)
providing a second region of a second conductivity type	P layer (4) lying over said N layer (2)
over said first region;	
providing a third region of said first conductivity type	N+ layer (5) lying above the P layer (4)
such that said first and third regions are separated by	
said second region;	
providing a trench through said third and second	trench (6) through the N+ layer (5) and the P layer (4)
regions; and	(0)
providing a gate in said trench;	metal gate layer (8)
wherein a portion P of said second region, which portion	a portion of the P layer (3) is spaced from the trench (6) and extends deeper than trench (6)
is spaced from said trench, extends deeper than said	and extends deeper than trench (6)
trench so that, if a predetermined voltage is applied to said gate and to said third region and another	
predetermined voltage is applied to said first region, an	
avalanche breakdown occurs away from a surface of	
said trench.	
CLAIM 18	
18. The method of claim 17 wherein said portion P of	a portion of the second region is doped P+ (3) which is
said second region is doped heavier than another portion	heavier doped than another portion of the second region
of said second region which portion is adjacent said	that is adjacent the trench (6)
trench.	
CLAIM 19	
19. The method of claim 17 wherein said first region	P+ layer (1) under N layer (2)
comprises a first portion and a second portion over said	
first portion, said second portion being lighter doped	
than said first portion.	
CLAIM 20	
20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
breakdown is a reach-through breakdown across said	across the N layer (2)
second portion.	
CLAIM 22	
21. The method of claim 17 further comprising the step	gate oxide (7)
of providing an insulator between said surface of said	
trench and said gate.	

CLAIM 23	
23. A method for providing a transistor, said method	VMOS FET
comprising the steps of:	
	See fig. 1
providing a first region of a first conductivity type;	
providing a second region of said first conductivity type	N layer (2)
over said first region, said second region being lighter	
doped than said first region;	
providing a third region of a second conductivity type	P layer (4)
	N+ layer (5) lying above the P layer (4)
	trench (6) through the N+ layer (5) and the P layer (4).
	metal gate layer (8)
	the deepest part of the P layer (3) is laterally spaced from
	trench (6)
	the distance between the deepest part of the P layer (3)
	and the P+ layer (1) is less than a depletion width of a
	planar junction which has the same doping profile as
	does the junction between the N layer (2) and the P layer
third regions at said deepest part of said third region and	(3) at the deepest part of the P layer (3) and which is reverse biased around its breakdown voltage
	reverse blased around its bleakdown voltage
	the deepest part of the third region is doped P+ (3) which
	is heavier doped than the part of the third region (4)
	adjacent the trench (6)
	adjacent me nemen (o)
	23. A method for providing a transistor, said method comprising the steps of: providing a first region of a first conductivity type; providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;

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U.S. Patent 5,072,266	JP 59-193064
CLAIM 1	
1. A trench DMOS transistor cell comprising:	VMOS FET
	See fig. 2
a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (3)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first covering layer;	P layer (4)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both vertically upward and downward, an upward portion	N+ layer (5) lying partly over the P layer (4), a portion of the P layer (4) extending vertically upward through the N+ layer (5) and downward into the N layer (3)

1	surface of the third covering layer and a downward portion extending downward into the first covering	·
2	layer;	
3	a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer	trench (1) having a bottom surface and side surfaces and extending vertically downward through the N+ layer (5), the P layer (4) and a portion of the N layer (3), where the
4	and the second covering layer and through a portion of	bottom surface of the trench (10 lies above the lowest
	the first covering layer, wherein the bottom surface of	portion of the P layer (4)
5	the trench lies above a lowest part of the downward	
	portion of the second covering layer;	
6	electrically conducting semiconductor material positioned within the trench;	gate semiconductor material (8) in trench (1)
7	a layer of oxide positioned within the trench between the	gate oxide (2)
	electrically conducting semiconductor material and the	
8	bottom and side surfaces of the trench; and	
9	three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering	gate (8), source (7) and drain (6)
	layer and to the substrate, respectively.	
10		· · · · · · · · · · · · · · · · · · ·

U.S. Patent No. 5,298,442	JP 59-193064
CLAIM 17	
17. A method for providing a transistor, said method	VMOS FET
comprising the steps of:	
	See fig. 2
providing a first region of a first conductivity type;	N+ layer and N layer (3)
providing a second region of a second conductivity type	P layer (4) over N layer (3)
over said first region;	
providing a third region of said first conductivity type	N+ layer (5) lying above the P layer (4).
such that said first and third regions are separated by	
said second region;	
providing a trench through said third and second regions; and	trench (1) through N+ layer (5) and P layer (4)
providing a gate in said trench;	coto comico dustas metalica (0)
wherein a portion P of said second region, which portion	gate semiconductor material (8)
is spaced from said trench, extends deeper than said	a portion of the P layer (4) is spaced from trench (1) an extends deeper than trench (1)
trench so that, if a predetermined voltage is applied to	extends deeper than bench (1)
said gate and to said third region and another	
predetermined voltage is applied to said first region, an	
avalanche breakdown occurs away from a surface of	
said trench.	
CLAIM 18	
18. The method of claim 17 wherein said portion P of	obvious to have the second region with a heavier doped
said second region is doped heavier than another portion	P+ portion
of said second region which portion is adjacent said	·
trench.	

1	CLAIM 19	
	19. The method of claim 17 wherein said first region	N+ layer under N- layer (3)
2	comprises a first portion and a second portion over said	, (-)
	first portion, said second portion being lighter doped	
3	than said first portion.	
	CLAIM 20	
4	20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
	breakdown is a reach-through breakdown across said	across the N- layer (3)
5	second portion.	
,	CLAIM 22	
6	21. The method of claim 17 further comprising the step	gate oxide (2)
7	of providing an insulator between said surface of said	
7	trench and said gate.	
8	CLAIM 23	
0	23. A method for providing a transistor, said method	VMOS FET
9	comprising the steps of:	·
		See fig. 2
10	providing a first region of a first conductivity type;	N+ layer
	providing a second region of said first conductivity type	N layer (3) lying above the N+ layer
11	over said first region, said second region being lighter	
•	doped than said first region;	
12	providing a third region of a second conductivity type	P layer (4)
	over said second region, said second and third regions	
13	forming a junction;	
	providing a fourth region of said first conductivity type	N+ layer (5) lying above the P layer (4)
14	over said third region;	
	providing a trench through said fourth region and third	trench (1) through the N+ layer (5) and P layer (4)
15	regions; and	11 (2)
	providing a gate in said trench;	gate oxide (2)
16	wherein a deepest part of said third regions is laterally	the deepest part of P layer (4) is laterally spaced from
	spaced from said trench;	trench (1)
17	wherein a distance between said deepest part of said	the distance between the deepest part of the P layer (4)
10	third region and said first region is less than a depletion width of a planar junction which has the same doping	and the N+ layer is less than a depletion width of a planar
18	profile as does said junction between said second and	junction which has the same doping profile as does the
19	third regions at said deepest part of said third region and	junction between the N- layer (3) and the P layer (4) at
19	which is reverse biased around its breakdown voltage.	the deepest part of the P layer (4) and which is reverse
20	. CLAIM 24	biased around its breakdown voltage
20	24. The method of claim 23 wherein said deepest part of	abyrious to have the second series with the
21	said third region is doped heavier than a part of said	obvious to have the second region with a heavier doped
~ 1	third region which part is adjacent said trench.	P+ portion laterally spaced from the trench (1)
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U.S. Patent 5,072,266	JP 60-28271
CLAIM 1	
. A trench DMOS transistor cell comprising:	VMOSFET
	See fig. 3(a-h)
a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (1)

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. 1	a first covering layer of semiconductor material of said	N layer (2)
2	first electrical conductivity type lying on the substrate;	
2	a second covering layer of semiconductor material of	P layer (8) and (11)
3	second electrical conductivity type lying on the first	
3	covering layer;	
4	a third covering layer of semiconductor material of	N+ layer (9) lying partly over the P layer (8), where a
4	heavily doped said first electrical conductivity type and	portion of the P layer (11) extends vertically upward
5	having a top surface and partly lying over the second	through the N+ layer
)	covering layer, wherein a portion of the second covering	
6	layer is heavily doped and this portion extends both	
U	vertically upward and downward, an upward portion	
7	extending through the third covering layer to the top	*
,	surface of the third covering layer and a downward	
8	portion extending downward into the first covering	
٥	layer;	
9	a trench having a bottom surface and side surfaces and	trench (10) having a bottom surface and side surfaces and
9	extending vertically downward from the top surface of	extending vertically downward through the N+ layer (9)
10	the third covering layer through the third covering layer	and the P layer (8) and through a portion of the N layer
10	and the second covering layer and through a portion of	(2)
11	the first covering layer, wherein the bottom surface of	
11	the trench lies above a lowest part of the downward	
12	portion of the second covering layer;	
	electrically conducting semiconductor material positioned within the trench:	poly gate (6) in trench (10)
13		
13	a layer of oxide positioned within the trench between the	gate oxide film (5)
14	electrically conducting semiconductor material and the	
17	bottom and side surfaces of the trench; and	
15	three electrodes electrically coupled to the electrically	gate (6), source (14) and drain (backside)
	conducting semiconductor material, to the third covering	
16	layer and to the substrate, respectively.	

U.S. Patent No. 5,298,442	JP 60-28271
CLAIM 17	
7. A method for providing a transistor, said method comprising the steps of:	VMOSFET
-	See fig. 3(a-h)
providing a first region of a first conductivity type;	N+ layer (1) and N layer (2).
providing a second region of a second conductivity type over said first region;	P layer (8) and (11).
roviding a third region of said first conductivity type such that said first and third regions are separated by sid second region;	N+ layer (9) lying above the P layer (8).
roviding a trench through said third and second gions; and	trench (10) through N+ layer (9) and P layer (8)
roviding a gate in said trench;	poly gate (6) in trench (10)

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1	wherein a portion P of said second region, which portion	a portion P of the second region (11) is spaced from the trench (10);
2	is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to	
_	said gate and to said third region and another	the second region extends deeper than the trench (10)
3	predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of	
4	said trench.	
*	Salu ucuon.	
5		
	CLAIM 18	· ·
6	18. The method of claim 17 wherein said portion P of	portion P of the second region (11) is doped heavier than
7	said second region is doped heavier than another portion	another portion (8) which is adjacent the trench
	of said second region which portion is adjacent said	
8	trench. CLAIM 19	
	19. The method of claim 17 wherein said first region	N+ layer (1) under N layer (2)
9	comprises a first portion and a second portion over said	
	first portion, said second portion being lighter doped	
10	than said first portion.	·
11	CLAIM 20	1 d l l l l l l l l l l l l l l l l l l
••	20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
12	breakdown is a reach-through breakdown across said	across the N layer (2)
	second portion. CLAIM 22	
13	21. The method of claim 17 further comprising the step	gate oxide film (5)
	of providing an insulator between said surface of said	guto omao mm (o)
14	trench and said gate.	
15	CLAIM 23	X X
15	23. A method for providing a transistor, said method	VMOSFET
16	comprising the steps of:	
		See fig. 3(a-h)
17	providing a first region of a first conductivity type;	N+ layer (1)
	providing a second region of said first conductivity type	N layer (2)
18	over said first region, said second region being lighter	
19	doped than said first region; providing a third region of a second conductivity type	P layer (8)
17	over said second region, said second and third regions	
20	forming a junction;	
	providing a fourth region of said first conductivity type	N+ layer (9) lying above the P layer (8)
21	over said third region;	(2) 121 (2)
	providing a trench through said fourth region and third	trench (10) through N+ layer (9) and P layer (8)
22	regions; and	1 (6) in trough (10)
23	providing a gate in said trench;	poly gate (6) in trench (10) deepest part of the third region is laterally spaced from
23	wherein a deepest part of said third regions is laterally	the trench (10)
24	spaced from said trench; wherein a distance between said deepest part of said	the distance between the deepest part of the P layer (8)
- '	third region and said first region is less than a depletion	and the N+ layer (1) is less than a depletion width of a
25	width of a planar junction which has the same doping	planar junction which has the same doping profile as
	profile as does said junction between said second and	does the junction between the N- layer (2) and the P layer
26	third regions at said deepest part of said third region and	(8) at the deepest part of the P layer (8) and which is
	which is reverse biased around its breakdown voltage.	reverse biased around its breakdown voltage
27		

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SILICON VALLEY

ı	CLAIM 24	
ı	24. The method of claim 23 wherein said deepest part of	obvious to have deepest part of the third region doped
	said third region is doped heavier than a part of said	heavier than the part adjacent said trench
	third region which part is adjacent said trench.	

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5	INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266	
6	U.S. Patent 5,072,266	JP 57-18365
7	CLAIM 1	
7	1. A trench DMOS transistor cell comprising:	VMOS FET
8		
	a substante of seminar due to material of heavily do not	See fig. 2
9	a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (1)
10	a first covering layer of semiconductor material of said	N layer (2)
	first electrical conductivity type lying on the substrate;	71 (0)
11	a second covering layer of semiconductor material of second electrical conductivity type lying on the first	P layer (3)
	covering layer;	
12	a third covering layer of semiconductor material of	N+ layer (4) lying partly over the P layer (3)
13	heavily doped said first electrical conductivity type and	
	having a top surface and partly lying over the second	
14	covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both	
	vertically upward and downward, an upward portion	
15	extending through the third covering layer to the top	
16	surface of the third covering layer and a downward	
10	portion extending downward into the first covering	
17	layer;	
	a trench having a bottom surface and side surfaces and	trench (5) have a bottom surface and side surfaces which
18	extending vertically downward from the top surface of the third covering layer through the third covering layer	extend vertically downward through the N+ layer (4) and the P layer (3) and through a portion of the N layer (2)
	and the second covering layer and through a portion of	ate 1 rayor (5) and amough a portion of the 1 rayor (2)
19	the first covering layer, wherein the bottom surface of	in fig. 4, the P layer (2) lies between the N+ layer (4) and
20	the trench lies above a lowest part of the downward	the N layer (2) and extends below the bottom surface of
	portion of the second covering layer;	the trench (5)
21	electrically conducting semiconductor material	gate (7) in trench (5)
	positioned within the trench; a layer of oxide positioned within the trench between the	gate oxide layer between gate (7) and trench (5)
22	electrically conducting semiconductor material and the	gate oxide layer between gate (7) and trench (3)
23	bottom and side surfaces of the trench; and	·
23	three electrodes electrically coupled to the electrically	gate (7), source (6) and drain (not drawn)
24	conducting semiconductor material, to the third covering	
	layer and to the substrate, respectively.	·
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	U.S. Patent No. 5,298,442	JP 57-18365
ļ	CLAIM 17	
	17. A method for providing a transistor, said method	VMOS FET
	comprising the steps of:	
	providing a first ragion of a first and the	See fig. 2
	providing a first region of a first conductivity type; providing a second region of a second conductivity type	N+ layer (1) and N layer (2).
	over said first region;	P layer (3).
	providing a third region of said first conductivity type	N+ layer (4) lying above the P layer (3).
	such that said first and third regions are separated by	i tv layer (4) lying above the r layer (3).
	said second region;	
ſ	providing a trench through said third and second	trench (5) through N+ layer (4) and P layer (3)
ĺ	regions; and	
	providing a gate in said trench;	gate (7) in trench (5)
	wherein a portion P of said second region, which portion	the P layer (3) extends upward through the N+ layer (4
	is spaced from said trench, extends deeper than said	
	trench so that, if a predetermined voltage is applied to	in fig. 4, P layer (4) extends deeper than trench (5)
	said gate and to said third region and another	•
	predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of	
	said trench.	
ı		
1	CLAIM 18	
I	18. The method of claim 17 wherein said portion P of	obvious to have the second region with a heavier dopec
	said second region is doped heavier than another portion	P+ portion laterally spaced from the trench (1)
	of said second region which portion is adjacent said	·
	trench.	
Ĺ	CLAIM 19	
	19. The method of claim 17 wherein said first region	N+ layer (1) under N- layer (2)
ı	comprises a first portion and a second portion over said	
	first portion, said second portion being lighter doped	
L	than said first portion.	
-	CLAIM 20	
	20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said	avalanche breakdown is a reach-through breakdown across the N- layer (2)
	second portion.	across the 14- tayor (2)
۲	CLAIM 22	
۲	21. The method of claim 17 further comprising the step	gate oxide layer between gate (7) and trench (5)
	of providing an insulator between said surface of said	5
11	trench and said gate.	
	CLAIM 23	
	23. A method for providing a transistor, said method	VMOS FET
	comprising the steps of:	
L		See fig. 2
	providing a first region of a first conductivity type;	N+ layer (1)
	providing a second region of said first conductivity type	N layer (2)
	over said first region, said second region being lighter	
1	doped than said first region;	•

providing a third region of a second conductivity type over said second region, said second and third regions forming a junction; providing a fourth region of said first conductivity type over said third region; providing a trench through said fourth region and third regions; and providing a gate in said trench; wherein a deepest part of said third region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said deepest part of said third regions at said deepest part of said third regions at said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage CLAIM 24 24. The method of claim 23 wherein said deepest part of said third region which part is adjacent said trench. P layer (3) N+ layer (4) lying above the P layer (3) trench (5) through N+ layer (4) and P layer (3) deepest part of the third region is laterally spaced from the trench (5) the distance between the deepest part of the P layer (3) and the N+ layer (1) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer (2) and the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the		<u> </u>	
over said third region; providing a trench through said fourth region and third regions; and providing a gate in said trench; wherein a deepest part of said third regions is laterally spaced from said trench; wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage. 24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench trench (5) through N+ layer (4) and P layer (3) deepest part of the third region is laterally spaced from the trench (5) the distance between the deepest part of the P layer (3) and the N+ layer (1) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer (2) and the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) and which is reverse biased around its breakdown voltage CLAIM 24 24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench	1 2	over said second region, said second and third regions	P layer (3)
regions; and providing a gate in said trench; wherein a deepest part of said third regions is laterally spaced from said trench; wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer (2) and the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) and which is reverse biased around its breakdown voltage CLAIM 24 24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench	3	over said third region;	N+ layer (4) lying above the P layer (3)
wherein a deepest part of said third regions is laterally spaced from said trench; wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage. wherein a deepest part of the third region is laterally spaced from the trench (5) the distance between the deepest part of the P layer (3) and the N+ layer (1) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer (2) and the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the N- layer (2) and the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (1) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer (2) and the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) at the de	4		trench (5) through N+ layer (4) and P layer (3)
spaced from said trench; wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said trench deepest part of the third region is laterally spaced from the trench (5) the distance between the deepest part of the P layer (1) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer (2) and the P layer (3) at the deepest part of the P layer (3) and which is reverse biased around its breakdown voltage CLAIM 24 24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region with a heavier doped P+ portion laterally spaced from the trench (7)			gate (7) in trench (5)
third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region at said deepest part of said third region at said deepest part of said third region and which is reverse biased around its breakdown voltage. 10 the distance between the deepest part of the P layer (3) and the N+ layer (1) is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer (2) and the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) and which is reverse biased around its breakdown voltage CLAIM 24 24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench			deepest part of the third region is laterally spaced from the trench (5)
third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage. 10 third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does the junction between the N- layer (2) and the P layer (3) at the deepest part of the P layer (3) at the deepest part of the P layer (3) and which is reverse biased around its breakdown voltage CLAIM 24 24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench	6		the distance between the deepest part of the P layer (3)
profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage. CLAIM 24 24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench does the junction between the N- layer (2) and the P layer (3) at the deepest part of the P layer (3) and which is reverse biased around its breakdown voltage obvious to have the second region with a heavier doped P+ portion laterally spaced from the trench (7)	7	width of a planar junction which has the same doping	and the N+ layer (1) is less than a depletion width of a
which is reverse biased around its breakdown voltage. CLAIM 24 24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said third region which part is adjacent said trench reverse biased around its breakdown voltage obvious to have the second region with a heavier doped P+ portion laterally spaced from the trench (7)	8	third regions at said deepest part of said third region and	does the junction between the N- layer (2) and the P layer
said third region is doped heavier than a part of said third region which part is adjacent said trench P+ portion laterally spaced from the trench (7)	9		
11 unit region which part is adjacent said trench.	10	said third region is doped heavier than a part of said	obvious to have the second region with a heavier doped P+ portion laterally spaced from the trench (7)
	11	unru region which part is adjacent said french.	

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14	U.S. Patent 5,072,266	JP 59-80970	
	CLAIM 1		
15	1. A trench DMOS transistor cell comprising:	V Groove MOSFET	
16		See fig. 2	
17	a substrate of semiconductor material of heavily doped first electrical conductivity type;	N+ layer (2)	
18	a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	N layer (1)	
19	a second covering layer of semiconductor material of second electrical conductivity type lying on the first	P layer (8)	
	covering layer;	,	
20	a third covering layer of semiconductor material of	N+ layer (4) lying partly over the P layer (8), where the P	
	heavily doped said first electrical conductivity type and	layer (8) extends vertically upward through the N+ layer	
21	having a top surface and partly lying over the second	(4) and vertically downward into the N layer (1)	
	covering layer, wherein a portion of the second covering		
22	layer is heavily doped and this portion extends both		
	vertically upward and downward, an upward portion		
23	extending through the third covering layer to the top		
	surface of the third covering layer and a downward		
24	portion extending downward into the first covering layer;		
25	a trench having a bottom surface and side surfaces and	trench having a bottom surface and side surface, and	
	extending vertically downward from the top surface of	extending vertically downward through the N+ layer (4)	
26	the third covering layer through the third covering layer	and the P layer (8) and through a portion of the N layer	
	and the second covering layer and through a portion of	(1)	
27	the first covering layer, wherein the bottom surface of		
	the trench lies above a lowest part of the downward		
28	portion of the second covering layer;		
- 1	DOCSSV2-500277.1		

1	electrically conducting semiconductor material	gate (6) in trench
	positioned within the trench;	
2	a layer of oxide positioned within the trench between the	gate oxide layer (5)
	electrically conducting semiconductor material and the	
3	bottom and side surfaces of the trench; and	
	three electrodes electrically coupled to the electrically	gate (5), source (7) and drain (not drawn)
4	conducting semiconductor material, to the third covering	
	layer and to the substrate, respectively.	·
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7	INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442		
8	U.S. Patent No. 5,298,442	JP 59-80970	
	CLAIM 17		
.9	17. A method for providing a transistor, said method comprising the steps of:	V Groove MOSFET	
10	comprising the steps of :	See fig. 2	
11	providing a first region of a first conductivity type;	N+ layer (2) and N layer (1)	
12	providing a second region of a second conductivity type over said first region;	P layer (8)	
12	providing a third region of said first conductivity type	N+ layer (4) lying above the P layer (8)	
13	such that said first and third regions are separated by said second region;		
14	providing a trench through said third and second regions; and	trench through N+ layer (4) and P layer (8)	
15	providing a gate in said trench;	gate (6) in trench	
16	wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said	a portion of the P layer (8) is laterally spaced from the trench	
17	trench so that, if a predetermined voltage is applied to said gate and to said third region and another		
. 1 ′	predetermined voltage is applied to said first region, an	·	
18	avalanche breakdown occurs away from a surface of said trench.		
19			
-			
20	CLAIM 18		
21	18. The method of claim 17 wherein said portion P of	obvious to have the second region with a heavier doped P+ portion laterally spaced from the trench	
-1	said second region is doped heavier than another portion of said second region which portion is adjacent said	r+ portion laterary spaced from the trench	
22	trench.		
[CLAIM 19		
23	19. The method of claim 17 wherein said first region	N+ layer (2) under N- layer (1)	
24	comprises a first portion and a second portion over said first portion, said second portion being lighter doped		
	than said first portion.		
25	CLAIM 20		
26	20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said	avalanche breakdown is a reach-through breakdown across the N- layer (1)	
27	second portion.		

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1	CLAIM 22	
	21. The method of claim 17 further comprising the step	gate oxide layer (5)
2	of providing an insulator between said surface of said	
	trench and said gate.	
3	CLAIM 23	
	23. A method for providing a transistor, said method	V Groove MOSFET
4	comprising the steps of:	
_		See fig. 2
5	providing a first region of a first conductivity type;	N+ layer (2)
_	providing a second region of said first conductivity type	N layer (1)
6	over said first region, said second region being lighter	
7	doped than said first region;	
/	providing a third region of a second conductivity type	P layer (8)
8	over said second region, said second and third regions	
0	forming a junction;	·
9	providing a fourth region of said first conductivity type	N+ layer (4) lying above the P layer (8)
	over said third region;	
10	providing a trench through said fourth region and third	V trench extends through the N+ layer (4) and the P layer
	regions; and	(3)
11	providing a gate in said trench;	gate (6) in the V trench
	wherein a deepest part of said third regions is laterally	the deepest part of the P layer (8) is laterally spaced from
12	spaced from said trench;	the V trench
	wherein a distance between said deepest part of said	the distance between the deepest part of the P layer (8)
13	third region and said first region is less than a depletion width of a planar junction which has the same doping	and the N+ layer (2) is less than a depletion width of a
	profile as does said junction between said second and	planar junction which has the same doping profile as
14	third regions at said deepest part of said third region and	does the junction between the N-layer (1) and the P layer
	which is reverse biased around its breakdown voltage.	(8) at the deepest part of the P layer (8) and which is reverse biased around its breakdown voltage
15	CLAIM 24	reverse blased around its breakdown voltage
,	24. The method of claim 23 wherein said deepest part of	obvious to have the second region with a harrist 1
16	said third region is doped heavier than a part of said	obvious to have the second region with a heavier doped P+ portion laterally spaced from the trench
17	third region which part is adjacent said trench.	portion faterally spaced from the trench
1/		<u> </u>

INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,072,266 U-MOS Power FET, National Technical U.S. Patent 5,072,266 Report, Vol. 29(2), April 1983 CLAIM 1 1. A trench DMOS transistor cell comprising: U-MOSFET - see Fig. 3 Conceptional fabrication process of U-MOSFET a substrate of semiconductor material of heavily doped n+ layer first electrical conductivity type; a first covering layer of semiconductor material of said n- layer first electrical conductivity type lying on the substrate; a second covering layer of semiconductor material of p layer second electrical conductivity type lying on the first covering layer; a third covering layer of semiconductor material of n+ layer heavily doped said first electrical conductivity type and

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1	having a top surface and partly lying over the second covering layer, wherein a portion of the second covering	the p layer includes a p+ portion which extends upward through the n+ layer and downward into the n-layer
2	layer is heavily doped and this portion extends both vertically upward and downward, an upward portion	
3	extending through the third covering layer to the top surface of the third covering layer and a downward	
4	portion extending downward into the first covering layer;	•
5	a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of	trench with a bottom surface and side surfaces which extends downward from the top surface of the n+ layer
6	the third covering layer through the third covering layer and the second covering layer and through a portion of	through the n+ layer, the p layer and through a portion of the n- layer.
7	the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward	
8	portion of the second covering layer;	
	electrically conducting semiconductor material	semiconductor material within the trench
9	positioned within the trench;	
	a layer of oxide positioned within the trench between the	oxide positioned within the trench between the
10	electrically conducting semiconductor material and the	semiconductor material and the bottom and side surfaces
	bottom and side surfaces of the trench; and	of the trench
11	three electrodes electrically coupled to the electrically	three electrodes electrically coupled to the semiconductor
	conducting semiconductor material, to the third covering	material, to the top n+ layer and to the n+ substrate.
12	layer and to the substrate, respectively.	

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15	INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 5,298,442	
16		U-MOS Power FET, National Technical Report, Vol. 29(2), April 1983
17	CLAIM 17	
1/	17. A method for providing a transistor, said method	U-MOSFET – see Fig. 3 Conceptional fabrication
	comprising the steps of	process of U-MOSFET

comprising the steps of :	process of O-WOSI ET
providing a first region of a first conductivity type;	n+ layer substrate and n- layer
providing a second region of a second conductivity type over said first region;	p layer
providing a third region of said first conductivity type such that said first and third regions are separated by said second region;	n+ layer
providing a trench through said third and second regions; and	trench with a bottom surface and side surfaces which extend vertically downward through the n+ third region, and the p second region
providing a gate in said trench;	gate electrode in the trench
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said	the p second region has a heavily doped p+ region which is spaced from said trench and extends deeper than said

24	is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an
	trench so that, if a predetermined voltage is applied to
25	said gate and to said third region and another
	predetermined voltage is applied to said first region, an
26	avalanche breakdown occurs away from a surface of

trench

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said trench.

1	CLAIM 18	
	18. The method of claim 17 wherein said portion P of	the p second region contains a portion P which is doped
2	said second region is doped heavier than another portion	heavier than another portion of said second region which
	of said second region which portion is adjacent said	is adjacent said trench
3	trench.	
	CLAIM 19	
4	19. The method of claim 17 wherein said first region	the first region comprises a n+ layer substrate (first
	comprises a first portion and a second portion over said	portion) and a n- layer (second portion)
5	first portion, said second portion being lighter doped	
	than said first portion.	
6	CLAIM 20	
	20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
. 7	breakdown is a reach-through breakdown across said	across the n- layer (second portion) of the first region
	second portion.	
8	CLAIM 22	·
_	21. The method of claim 17 further comprising the step	oxide positioned within the trench between the
9	of providing an insulator between said surface of said	semiconductor material and the bottom and side surfaces
10	trench and said gate.	of the trench
10	CLAIM 23	
11	23. A method for providing a transistor, said method	U-MOSFET – see Fig. 3 Conceptional fabrication
11	comprising the steps of:	process of U-MOSFET
12	providing a first region of a first conductivity type;	n+ layer
	providing a second region of said first conductivity type	n- layer
13	over said first region, said second region being lighter	
	doped than said first region;	
14	providing a third region of a second conductivity type	p layer over n- layer
	over said second region, said second and third regions	•
15	forming a junction;	
	providing a fourth region of said first conductivity type	n+ layer formed over the p layer
16	over said third region;	4 1 4 1 (6 4
	providing a trench through said fourth region and third regions; and	trench extending downward through the n+ layer (fourth
17	providing a gate in said trench;	region) and the p layer (third region) gate electrode in the trench
10	wherein a deepest part of said third regions is laterally	the deepest part of the p layer (third region) is laterally
18	spaced from said trench;	spaced from the trench
19	wherein a distance between said deepest part of said	spaced from the deficit
17	third region and said first region is less than a depletion	•
20	width of a planar junction which has the same doping	-
	profile as does said junction between said second and	
21	third regions at said deepest part of said third region and	
-	which is reverse biased around its breakdown voltage.	
22	CLAIM 24	
	24. The method of claim 23 wherein said deepest part of	the deepest part of the p layer (third region) is doped
23	said third region is doped heavier than a part of said	heavier (p+) than the part of the p layer (third region)
	third region which part is adjacent said trench.	adjacent the trench
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U.S. Patent 5,		КАТОН
CLAIM		
1. A trench DMOS transistor cel	ll comprising:	Design of New Structural High Breakdown Voltage V- MOSFET—Static Shield V-MOSFET
		Fig. 3 Cross-sectional view and device parameters of SSV-MOSFET
a substrate of semiconductor ma first electrical conductivity type;		n+ layer
a first covering layer of semicon first electrical conductivity type	lying on the substrate;	n- layer
a second covering layer of semic second electrical conductivity ty covering layer;	onductor material of pe lying on the first	p layer
a third covering layer of semicon heavily doped said first electrical having a top surface and partly ly	conductivity type and ring over the second	n+ layer
covering layer, wherein a portion layer is heavily doped and this po	ortion extends both	
vertically upward and downward extending through the third cover surface of the third covering laye	ring layer to the top	
portion extending downward into layer;	the first covering	
a trench having a bottom surface	and side surface 1	
extending vertically downward fr the third covering layer through the	om the top surface of	trench extends downward from the top surface of the n+ layer through the n+ layer, the p layer and through a portion of the n- layer.
and the second covering layer and the first covering layer, wherein the	I through a portion of he bottom surface of	
the trench lies above a lowest part portion of the second covering lay	t of the downward ver;	
electrically conducting semicondupositioned within the trench;		semiconductor material within the trench
a layer of oxide positioned within electrically conducting semicondu	ctor material and the	oxide positioned within the trench between the semiconductor material and the bottom and side surface:
bottom and side surfaces of the tre	ench; and	of the trench
three electrodes electrically couple conducting semiconductor materia layer and to the substrate, respecti	al, to the third covering	three electrodes electrically coupled to the semiconducto material, to the top n+ layer and to the n+ substrate.

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U.S. Patent No. 5,298,442	КАТОН
CLAIM 17	
17. A method for providing a transistor, said method	Design of New Structural High Breakdown Voltage V
comprising the steps of:	MOSFET—Static Shield V-MOSFET
	Fig. 1.C. and the second of th
	Fig. 3 Cross-sectional view and device parameters of SSV-MOSFET
providing a first region of a first conductivity type;	n+ layer substrate and n- layer
providing a second region of a second conductivity type	p layer
over said first region;	
providing a third region of said first conductivity type	n+ layer
such that said first and third regions are separated by	
said second region;	
providing a trench through said third and second	trench extends through the n+ layer (third region) and
regions; and	p layer (second region)
providing a gate in said trench;	gate electrode in the trench
wherein a portion P of said second region, which portion	the p second region has a portion which is spaced from
is spaced from said trench, extends deeper than said	said trench and extends deeper than said trench
trench so that, if a predetermined voltage is applied to said gate and to said third region and another	_
predetermined voltage is applied to said first region, an	
avalanche breakdown occurs away from a surface of	' ·
said trench.	
CLAIM 18	
18. The method of claim 17 wherein said portion P of	N/A
said second region is doped heavier than another portion	
of said second region which portion is adjacent said	
trench.	
CLAIM 19	
19. The method of claim 17 wherein said first region	the first region comprises a n+ layer substrate (first
comprises a first portion and a second portion over said	portion) and a n- layer (second portion)
first portion, said second portion being lighter doped than said first portion.	
CLAIM 20	
20. The method of claim 19 wherein said avalanche	avalanche breakdown is a reach-through breakdown
breakdown is a reach-through breakdown across said	across the n- layer (second portion) of the first region
second portion.	, (, , , , , , , , , , , , , , , , , ,
CLAIM 22	-7-
21. The method of claim 17 further comprising the step	oxide positioned within the trench between the
of providing an insulator between said surface of said	semiconductor material and the bottom and side surface
trench and said gate.	of the trench
CLAIM 23	
	Design of New Structural High Breakdown Voltage V-
23. A method for providing a transistor, said method	
	MOSFET—Static Shield V-MOSFET
23. A method for providing a transistor, said method	MOSFET—Static Shield V-MOSFET
23. A method for providing a transistor, said method	

	providing a second region of said first conductivity type	n- layer
	over said first region, said second region being lighter	
	doped than said first region;	·
١	providing a third region of a second conductivity type	p layer over n- layer
- 1	over said second region, said second and third regions	
	forming a junction;	
	providing a fourth region of said first conductivity type	n+ layer formed over the p layer
l	over said third region;	• •
	providing a trench through said fourth region and third	trench extending downward through the n+ layer (fourth
	regions; and	region) and the p layer (third region)
	providing a gate in said trench;	gate electrode in the trench
	wherein a deepest part of said third regions is laterally	the deepest part of the p layer (third region) is laterally
	spaced from said trench;	spaced from the trench
	wherein a distance between said deepest part of said	
	third region and said first region is less than a depletion	
	width of a planar junction which has the same doping	
	profile as does said junction between said second and	
	third regions at said deepest part of said third region and	
1	which is reverse biased around its breakdown voltage.	
Ļ	CLAIM 24	
ı	24. The method of claim 23 wherein said deepest part of	N/A
	said third region is doped heavier than a part of said	
	third region which part is adjacent said trench.	
ti		· · · · · · · · · · · · · · · · · · ·

Prior Art Under 35 U.S.C. § 103 Which Render the '266 and '442 Patents Obvious:

U.S. Patent 4,345,265 in combination with U.S. Patent 4,374,455

U.S. Patent 4,443,931 in combination with U.S. Patent 4,374,455

U.S. Patent 4,532,534 in combination with U.S. Patent 4,374,455

U.S. Patent 4,345,265 in combination with U.S. Patent 4,767,722

U.S. Patent 4,783,694 in combination with U.S. Patent 3,412,297

U.S. Patent 4,593,302 in combination with U.S. Patent 3,412,297

(Multiple alternative combinations using the prior art references combined above can be made which additionally render the '266 and '442 patents obvious)

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SILICON VALLEY

_	INVALIDITY CLAIM CHART FOI	
2	U.S. Patent 5,072,266	U.S. Patent 4,345,265 In Combination With U.S. Patent 4,374,455
	CLAIM 1	
4 5	1. A trench DMOS transistor cell comprising:	'265 Patent: MOS Power Transistor With Improved- High-Voltage Capability
6		'455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
7	a substrate of semiconductor material of heavily doped first electrical conductivity type;	'265 Patent: Figs. 4-6: N+ layer (10) '455 Patent: Fig. 2: N+ layer (34)
8	a first covering layer of semiconductor material of said	'265 Patent: Figs. 4-6: N- layer (12)
	first electrical conductivity type lying on the substrate;	(455 D
9	a second covering layer of semiconductor material of	'455 Patent: Fig. 2: N- layer (36) '265 Patent: Figs. 4-6: P- layer (20), (21), (22) and (23)
10	second electrical conductivity type lying on the first covering layer;	
11		'455 Patent: Fig. 2: P layer (52) and (54)
12	a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and	'265 Patent: Figs. 4-6: N+ layer (32) and (34) partly lying over P- layer (20) and (22).
13	having a top surface and partly lying over the second covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both	'265 Patent: Figs. 4-6: a portion of the P- layer is a heavily doped P+ region (21) and (23) and extends both
14	vertically upward and downward, an upward portion	vertically upward and downward; an upward portion of
15	extending through the third covering layer to the top surface of the third covering layer and a downward	the P+ region extends through the N+ layer (32) and (34) and a downward portion extends downward into the N-layer (12).
16	portion extending downward into the first covering layer;	'455 Patent: Fig. 2: N+ layer (40) partly lying over P
17		layer (52) and (54)
18		'455 Patent: Fig. 2: a portion of the P layer (52) is a heavily doped P+ region (54) and extends both vertically upward and downward; an upward portion of the P+
19		region extends through the N+ layer (40) and a downward portion extends downward in the N- layer
20		(36).
21	a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of the third covering layer through the third covering layer	'455 Patent: Fig. 2: groove (42) having a bottom surface and side surfaces and extending vertically downward from the N+ layer (40) through the N+ layer (40) and the
22	and the second covering layer and through a portion of the first covering layer, wherein the bottom surface of	P layer (52) and through a portion of the N- layer (36).
23	the trench lies above a lowest part of the downward portion of the second covering layer;	'265 patent and '455 patent: the deep P+ region (21) and (23) of the '265 patent would be below the lowest point
24	electrically conducting semiconductor material	of the grove (42) of the '455 patent '455 Patent: Fig. 2: electrode (49)
25	positioned within the trench; a layer of oxide positioned within the trench between the	'455 Patent: Fig. 2: oxide layer (47) within the groove
26	electrically conducting semiconductor material and the bottom and side surfaces of the trench; and	(42)
27	three electrodes electrically coupled to the electrically conducting semiconductor material, to the third covering	'455 Patent: Fig. 2: source electrodes (58), drain electrode (50) and gate electrode (49).
28	layer and to the substrate, respectively.	

1	INVALIDITY CLAIM CHART FOR	R U.S. PATENT NO. 5,298,442
2 3	U.S. Patent No. 5,298,442	U.S. Patent 4,345,265 In Combination With U.S. Patent 4,374,455
Ī	CLAIM 17	
4 5	17. A method for providing a transistor, said method comprising the steps of:	'265 Patent: MOS Power Transistor With Improved High-Voltage Capability
6		'455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
7	providing a first region of a first conductivity type;	'265 Patent: Figs. 4-6: N+ layer (10) and N- layer (12)
8	providing a second region of a second conductivity type over said first region;	'455 Patent: Fig. 2: N+ layer (34) and N- layer (36) '265 Patent: Figs. 4-6: P- layer (20), (21), (22) and (23); Col. 3, ln. 42.
9		'455 Patent: Fig. 2: P layer (52) and (54)
10	providing a third region of said first conductivity type such that said first and third regions are separated by	'265 Patent: Figs. 4-6: N+ layer (32) and (34) partly lying over P- layer (20) and (22).
11	said second region;	'455 Patent: Fig. 2: N+ layer (40)
12	providing a trench through said third and second regions; and	'455 Patent: Fig. 2: groove (42) extending vertically downward through the N+ layer (40) and the P layer (52)
13	providing a gate in said trench;	'455 Patent: Fig. 2: gate electrode (49) in groove (42)
14	wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said	'265 Patent: Col. 5, Ins. 32-47 - "The effect of regions 21 and 23 in enhancing the breakdown characteristic of the
15	trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an	DMOS structure comes about in several ways. First, the fact that the breakdown occurs at the external periphery of or beneath regions 21 and 22 diverts breakdown from
16	avalanche breakdown occurs away from a surface of said trench.	the sensitive channel regions of the DMOS device in the P- regions under the gate 24."
17 18	·	'265 patent and '455 patent: the deep P+ region (21) and (23) of the '265 patent would be below the lowest point of the grove (42) of the '455 patent
	CLAIM 18	
19	18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion	'455 Patent: Fig. 2: a portion of the P layer (52) is a heavily doped P+ region (54) and extends both vertically upward and downward; an upward portion of the P+
21	of said second region which portion is adjacent said trench.	region extends through the N+ layer (40) and a downward portion extends downward in the N- layer
22		(36).
23		'265 Patent: Figs. 4-6: a portion of the P- layer is a heavily doped P+ region (21) and (23) and extends both vertically upward and downward; P+ region (21) and
24		(23) are more heavily doped than P- region (20) and (22) near the gate region.
25	CLAIM 19	1455 patents Fig. 2: NJ Javar (24) under NJ Javar (25)
26	19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped	'455 patent: Fig. 2: N+ layer (34) under N- layer (36) '265 Patent: Figs. 4-6: N+ layer (10) under N- layer (12)
27	than said first portion.	

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1	CLAIM 20	
	20. The method of claim 19 wherein said avalanche	'265 Patent and '455 Patent: avalanche breakdown
2	breakdown is a reach-through breakdown across said	would be a reach-through breakdown across the N- layer
	second portion.	(12)
3	CLAIM 22	
Ì	21. The method of claim 17 further comprising the step	'455 Patent: oxide (47)
4	of providing an insulator between said surface of said	
- 1	trench and said gate.	
5	CLAIM 23	
	23. A method for providing a transistor, said method	'265 Patent: MOS Power Transistor With Improved
6	comprising the steps of:	High-Voltage Capability
-		
7		'455 Patent: Method for Manufacturing a Vertical,
		Grooved MOSFET
8	providing a first region of a first conductivity type;	'265 Patent: Figs. 4-6: N+ layer (10)
9		'455 Patent: Fig. 2: N+ layer (34)
_ [providing a second region of said first conductivity type	'265 Patent: Figs. 4-6: N- layer (12)
10	over said first region, said second region being lighter	
	doped than said first region;	'455 Patent: Fig. 2: N- layer (36)
11	providing a third region of a second conductivity type	'265 Patent: Figs. 4-6: P- layer (20), (21), (22) and (23)
	over said second region, said second and third regions	over the second region
12	forming a junction;	(455 D
.,		'455 Patent: Fig. 2: P layer (52)
13	providing a fourth region of said first conductivity type	'265 Patent: Figs. 4-6: N+ layer (32) and (34) partly lying over P- layer (20) and (22).
14	over said third region;	lying over F- layer (20) and (22).
14		'455 Patent: Fig. 2: N+ layer (40) partly lying over P
15	·	layer (52)
15	providing a trench through said fourth region and third	'455 Patent: Fig. 2: groove (42) through the N+ layer
16	regions; and	(40) and the P layer (52)
.	providing a gate in said trench;	'455 Patent: Fig. 2: gate electrode (49)
17	wherein a deepest part of said third regions is laterally	'265 Patent: Figs. 4-6: P+ region (21) and (23) is
1	spaced from said trench;	laterally spaced from the gate
18	wherein a distance between said deepest part of said	'265 and '455: a distance between said deepest part of a
	third region and said first region is less than a depletion	third region and a first region would be less than a
19	width of a planar junction which has the same doping	depletion width of a planar junction which has the same
	profile as does said junction between said second and	doping profile as does said junction between a second
20	third regions at said deepest part of said third region and	and third regions at said deepest part of the third region
	which is reverse biased around its breakdown voltage.	and which is reverse biased around its breakdown
21	Š	voltage.
	CLAIM 24	
22	24. The method of claim 23 wherein said deepest part of	'265 Patent: Figs. 4-6: a portion of the P- layer is a
	said third region is doped heavier than a part of said	heavily doped P+ region (21) and (23) and extends both
23	third region which part is adjacent said trench.	vertically upward and downward; P+ region (21) and
	' '	(23) are more heavily doped than P- region (20) and (22)
24	V V	(25) Me more heavily deped than 1 region (26) and (22)

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	U.S. Patent 5,072,266	U.S. Patent 4,443,931 In Combination With U.S. Patent 4,374,455
L	CLAIM 1	
1	I. A trench DMOS transistor cell comprising:	'931 Patent: Method of Fabricating a Semiconductor Device With a Base Region Having a Deep Portion
L		'455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
a fi	substrate of semiconductor material of heavily doped irst electrical conductivity type;	'931 Patent: Fig. 13: N+ layer (12)
2	first covering layer of semiconductor material of said	'455 Patent: Fig. 2: N+ layer (34)
fi	irst electrical conductivity type lying on the substrate;	'931 Patent: Fig. 13: N layer (14)
L	<u> </u>	'455 Patent: Fig. 2: N- layer (36)
a	second covering layer of semiconductor material of	'931 Patent: Fig. 13: P layer (34) and (28)
se	econd electrical conductivity type lying on the first	S ==== (0.1) and (20)
	overing layer;	'455 Patent: Fig. 2: P layer (52) and (54)
he	third covering layer of semiconductor material of eavily doped said first electrical conductivity type and	'931 Patent: Fig. 13: N+ layer (36) partly lying over layer (34) and (28).
ha	aving a top surface and partly lying over the second	
CC	overing layer, wherein a portion of the second covering	'931 Patent: Fig. 13: a portion of the P layer (34) is a
la	yer is heavily doped and this portion extends both	heavily doped P+ region (28) and extends both vertical
VE	ertically upward and downward, an upward portion	upward and downward; an upward portion of the P+
ex	stending through the third covering layer to the top	region extends through the N+ layer (38) and a
su	urface of the third covering layer and a downward	downward portion extends downward into the N layer (14).
	ortion extending downward into the first covering	(14).
la:	yer;	'455 Patent: Fig. 2: N+ layer (40) partly lying over P
		layer (52) and (54)
		'455 Patent: Fig. 2: a portion of the P layer (52) is a heavily doped P+ region (54) and extends both vertica
		upward and downward; an upward portion of the P+ region extends through the N+ layer (40) and a
		downward portion extends downward to the N- layer (36).
ex	trench having a bottom surface and side surfaces and tending vertically downward from the top surface of a third covering layer through the third covering layer through the third.	'455 Patent: Fig. 2: groove (42) having a bottom surfa and side surfaces and extending vertically downward
an	d the second covering layer and through a portion of	from the N+ layer (40) through the N+ layer (40) and P layer (52) and through a portion of the N- layer (36).
the	e first covering layer, wherein the bottom surface of e trench lies above a lowest part of the downward rtion of the second covering layer;	
ر <u>ان بر</u> مام	retrically conducting associated	1155
pos	ectrically conducting semiconductor material sitioned within the trench;	'455 Patent: Fig. 2: electrode (49)
a la	ayer of oxide positioned within the trench between the	'455 Patent: Fig. 2: oxide layer (47) within the groove
ele L-	ectrically conducting semiconductor material and the	(42)
001	ttom and side surfaces of the trench; and	
ur	ree electrodes electrically coupled to the electrically	'455 Patent: Fig. 2: source electrodes (58), drain
COL	nducting semiconductor material, to the third covering	electrode (50) and gate electrode (49).

U.S. Patent No. 5,298,442	U.S. Patent 4,443,931 In Combination With U.S. Patent 4,374,455
CLAIM 17	
17. A method for providing a transistor, said method comprising the steps of:	'931 Patent: Method of Fabricating a Semiconductor Device With a Base Region Having a Deep Portion
	'455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
providing a first region of a first conductivity type;	'931 Patent: Fig. 13: N+ layer (12) and N layer (14)
providing a second region of a second conductivity type	'455 Patent: Fig. 2: N+ layer (34) and N- layer (36) '931 Patent: Fig. 13: P layer (34) and (28)
over said first region;	'455 Patent: Fig. 2: P layer (52)
providing a third region of said first conductivity type	'931 Patent: Fig. 13: N+ layer (12) partly lying over P
such that said first and third regions are separated by said second region;	layer (34)
	'455 Patent: Fig. 2: N+ layer (40)
providing a trench through said third and second regions; and	'455 Patent: Fig. 2: groove (42) extending vertically downward through the N+ layer (40) and the P layer (52)
providing a gate in said trench;	'455 Patent: Fig. 2: gate electrode (49) in groove (42)
wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said	'931 patent and '455 patent: the deep P+ region (28) of the '931 patent would be below the lowest point of the
trench so that, if a predetermined voltage is applied to said gate and to said third region and another	grove (42) of the '455 patent
predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of	
said trench.	
CLAIM 18	
18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion	'931 Patent: Fig. 13: a portion of the P layer (34) is a heavily doped P+ region (28)
of said second region which portion is adjacent said trench.	'455 Patent: Fig. 2: a portion of the P layer (52) is a heavily doped P+ region (54) and extends both verticall
	upward and downward; an upward portion of the P+ region extends through the N+ layer (40) and a
-	downward portion extends downward in the N- layer (36).
CLAIM 19	
19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said	'455 patent: Fig. 2: N+ layer (34) under N- layer (36)
first portion, said second portion being lighter doped	'931 Patent: Fig. 13: N+ layer (12) under N- layer (14)
than said first portion.	
CLAIM 20	
20. The method of claim 19 wherein said avalanche	'931 Patent and '455 Patent: avalanche breakdown
breakdown is a reach-through breakdown across said	would be a reach-through breakdown across the N- laye
second portion.	(12)

	11	
1	CLAIM 22	
	21. The method of claim 17 further comprising the step	'455 Patent: oxide (47)
2	of providing an insulator between said surface of said	
	trench and said gate.	
3	CLAIM 23	
	23. A method for providing a transistor, said method	'931 Patent: Method of Fabricating a Semiconductor
4	comprising the steps of:	Device With a Base Region Having a Deep Portion
5		'455 Patent: Method for Manufacturing a Vertical,
		Grooved MOSFET
6	providing a first region of a first conductivity type;	'931 Patent: Fig. 13: N+ layer (12)
~		
7		'455 Patent: Fig. 2: N+ layer (34)
0	providing a second region of said first conductivity type	'931 Patent: Fig. 13: N layer (14)
8	over said first region, said second region being lighter	'455 Patent: Fig. 2: N- layer (36)
9	doped than said first region;	'931 Patent: Fig. 13: P layer (34) and (28)
9	providing a third region of a second conductivity type	931 Patent: Fig. 13: P layer (34) and (28)
10	over said second region, said second and third regions forming a junction;	'455 Patent: Fig. 2: P layer (52)
	providing a fourth region of said first conductivity type	'931 Patent: Fig. 13: N+ layer (36) partly lying over P
11	over said third region;	layer (34) and (28)
	over said time region,	
12	, and the second	'455 Patent: Fig. 2: N+ layer (40) partly lying over P
		layer (52)
13	providing a trench through said fourth region and third	'455 Patent: Fig. 2: groove (42) through the N+ layer
	regions; and	(40) and the P layer (52)
14	providing a gate in said trench;	'455 Patent: Fig. 2: gate electrode (49)
	wherein a deepest part of said third regions is laterally	'931 Patent: Fig. 13: P+ region (28) is laterally spaced
15	spaced from said trench;	from the gate
	wherein a distance between said deepest part of said	'931 and '455: a distance between said deepest part of a
16	third region and said first region is less than a depletion	third region and a first region would be less than a
17	width of a planar junction which has the same doping	depletion width of a planar junction which has the same
1/	profile as does said junction between said second and	doping profile as does said junction between a second
18	third regions at said deepest part of said third region and	and third regions at said deepest part of the third region
10	which is reverse biased around its breakdown voltage.	and which is reverse biased around its breakdown
19	CLAIM 24	voltage.
		'931 Patent: Fig. 13: a portion of the Player is a heavily
20	24. The method of claim 23 wherein said deepest part of said third region is doped heavier than a part of said	doped P+ region (28) and extends both vertically upward
	third region which part is adjacent said trench.	and downward; P+ region (28) is more heavily doped
21	ding region which part is adjacent said dencil.	than P- region (34) near the gate region.
		1 man 1 - region (34) near are gate region.

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SILICON VALLEY

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2	U.S. Patent 5,072,266	U.S. Patent 4,532,534 In Combination With U.S. Patent4,374,455
1	CLAIM 1	0.0.1 acone 1,0 / 1,100
	1. A trench DMOS transistor cell comprising:	'534 Patent: MOSFET With Perimeter Channel
;		'455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
	a substrate of semiconductor material of heavily doped first electrical conductivity type;	'534 Patent: Fig. 2: N+ layer (118)
,		'455 Patent: Fig. 2: N+ layer (34)
	a first covering layer of semiconductor material of said	'534 Patent: Fig. 2: N- layer (120)
3	first electrical conductivity type lying on the substrate;	'455 Patent: Fig. 2: N- layer (36)
	1	'534 Patent: Fig. 2: P layer (124) and (126)
)	a second covering layer of semiconductor material of second electrical conductivity type lying on the first	
).	covering layer;	'455 Patent: Fig. 2: P layer (52) and (54)
	a third covering layer of semiconductor material of	'534 Patent: Fig. 2: N+ layer (128) partly lying over P
i	heavily doped said first electrical conductivity type and	layer (124) and (126)
	having a top surface and partly lying over the second	'534 Patent: Fig. 2: a portion of the P layer is a heavily
?	covering layer, wherein a portion of the second covering	doped P+ region (126) and extends both vertically
	layer is heavily doped and this portion extends both	upward and downward; an upward portion of the P+
,	vertically upward and downward, an upward portion	region extends through the N+ layer (128) and a
	extending through the third covering layer to the top	downward portion extends downward into the N- layer
	surface of the third covering layer and a downward	(120).
	portion extending downward into the first covering	
;	layer;	'455 Patent: Fig. 2: N+ layer (40) partly lying over P layer (52) and (54)
5		C.1 D.1 (50)
7		'455 Patent: Fig. 2: a portion of the P layer (52) is a heavily doped P+ region (54) and extends both vertically upward and downward; an upward portion of the P+
	•	region extends through the N+ layer (40) and a
3	·	downward portion extends downward to the N- layer
•		(36).
,	a trench having a bottom surface and side surfaces and	'455 Patent: Fig. 2: groove (42) having a bottom surface
)	extending vertically downward from the top surface of	and side surfaces and extending vertically downward
•	the third covering layer through the third covering layer	from the N+ layer (40) through the N+ layer (40) and the
l	and the second covering layer and through a portion of	P layer (52) and through a portion of the N- layer (36).
-	the first covering layer, wherein the bottom surface of	
2	the trench lies above a lowest part of the downward	
	portion of the second covering layer;	
3	electrically conducting semiconductor material	'455 Patent: Fig. 2: electrode (49)
	positioned within the trench;	
ļ	a layer of oxide positioned within the trench between the	'455 Patent: Fig. 2: oxide layer (47) within the groove
	electrically conducting semiconductor material and the	(42)
5	bottom and side surfaces of the trench; and	
	three electrodes electrically coupled to the electrically	'455 Patent: Fig. 2: source electrodes (58), drain
5	conducting semiconductor material, to the third covering	electrode (50) and gate electrode (49).
	layer and to the substrate, respectively.	

1	INVALIDITY CLAIM CHART FOR	R U.S. PATENT NO. 5,298,442
2 3	U.S. Patent No. 5,298,442	U.S. Patent 4,443,534 In Combination With U.S. Patent 4,374,455
_	CLAIM 17	
4	17. A method for providing a transistor, said method comprising the steps of:	'534 Patent: MOSFET With Perimeter Channel
5		'455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
6	providing a first region of a first conductivity type;	'534 Patent: Fig. 2: N+ layer (118) and N layer (120)
7		'455 Patent: Fig. 2: N+ layer (34) and N- layer (36) '534 Patent: Fig. 2: P layer (124) and (126)
8	providing a second region of a second conductivity type over said first region;	'455 Patent: Fig. 2: P layer (52)
}		'534 Patent: Fig. 2: N+ layer (128) partly lying over P
9	providing a third region of said first conductivity type such that said first and third regions are separated by	layer (124) and (126)
10	said second region;	'455 Patent: Fig. 2: N+ layer (40)
11	providing a trench through said third and second regions; and	'455 Patent: Fig. 2: groove (42) extending vertically downward through the N+ layer (40) and the P layer (52)
.,	providing a gate in said trench;	'455 Patent: Fig. 2: gate electrode (49) in groove (42)
12 13	wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said	'534 patent and '455 patent: the deep P+ region (126) of the '534 patent would be below the lowest point of the- grove (42) of the '455 patent
14	trench so that, if a predetermined voltage is applied to said gate and to said third region and another	grove (42) of the 433 patent
15	predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of	·
16	said trench.	
17	CLAIM 18	
18	18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion	'534 Patent: Fig. 12: a portion of the P layer is a heavily doped P+ region (126)
19	of said second region which portion is adjacent said trench.	'455 Patent: Fig. 2: a portion of the P layer (52) is a
20	,	heavily doped P+ region (54) and extends both vertically upward and downward; an upward portion of the P+ region extends through the N+ layer (40) and a
21		downward portion extends downward in the N- layer (36).
22	CLAIM 19 19. The method of claim 17 wherein said first region	'455 patent: Fig. 2: N+ layer (34) under N- layer (36)
23	comprises a first portion and a second portion over said	'534 Patent: Fig. 2: N+ layer (118) under N- layer (120)
24	first portion, said second portion being lighter doped than said first portion.	33.12.102.11 1.g. 2.11 1.g. (1.11)
24	CLAIM 20	
25	20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said	'534 Patent and '455 Patent: avalanche breakdown would be a reach-through breakdown across the N- layer
26	second portion.	

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- 1		
1	CLAIM 22	
	21. The method of claim 17 further comprising the step	'455 Patent: oxide (47)
2	of providing an insulator between said surface of said	
	trench and said gate.	
3	CLAIM 23	
	23. A method for providing a transistor, said method	'534 Patent: Method of Fabricating a Semiconductor
4	comprising the steps of:	Device With a Base Region Having a Deep Portion
5		'455 Patent: Method for Manufacturing a Vertical, Grooved MOSFET
_		
6	providing a first region of a first conductivity type;	'534 Patent: Fig. 2: N+ layer (118)
7		'455 Patent: Fig. 2: N+ layer (34)
′	1	'534 Patent: Fig. 2: N- layer (120)
8	providing a second region of said first conductivity type	JUT Latent. Tig. 2. 13- layer (120)
٥	over said first region, said second region being lighter	'455 Patent: Fig. 2: N- layer (36)
_	doped than said first region;	'534 Patent: Fig. 2: P layer (124) and (126)
. 9	providing a third region of a second conductivity type	334 Patent: Fig. 2: P layer (124) and (126)
.,	over said second region, said second and third regions	'455 Patent: Fig. 2: P layer (52)
10	forming a junction;	
	providing a fourth region of said first conductivity type	'534 Patent: Fig. 2: N+ layer (128) partly lying over P
11	over said third region;	layer (124) and (126)
		'455 Patent: Fig. 2: N+ layer (40) partly lying over P
12		layer (52)
13	providing a trench through said fourth region and third	'455 Patent: Fig. 2: groove (42) through the N+ layer
13	regions; and	(40) and the P layer (52)
14		'455 Patent: Fig. 2: gate electrode (49)
14	providing a gate in said trench;	'534 Patent: Figs. 4-6: P+ region (126) is laterally
15	wherein a deepest part of said third regions is laterally	spaced from the gate
13	spaced from said trench;	
16	wherein a distance between said deepest part of said	'534 and '455: a distance between said deepest part of a
10	third region and said first region is less than a depletion	third region and a first region would be less than a depletion width of a planar junction which has the same
17	width of a planar junction which has the same doping	doping profile as does said junction between a second
17	profile as does said junction between said second and	
10	third regions at said deepest part of said third region and	and third regions at said deepest part of the third region and which is reverse biased around its breakdown
18	which is reverse biased around its breakdown voltage.	voltage.
19	CLAIM 24	
	24. The method of claim 23 wherein said deepest part of	'534 Patent: Figs. 4-6: a portion of the P layer is a
20	said third region is doped heavier than a part of said	heavily doped P+ region (126) and extends both
	third region which part is adjacent said trench.	vertically upward and downward; P+ region (126) is
21	mine radion timen have in adjacant pere grana.	more heavily doped than P region (124) which is near the
		gate region.
22		J G G

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U.S. Patent 5,072,266	U.S. Patent 4,345,265 In Combination With U.S. Patent 4,767,722
CLAIM 1	·
1. A trench DMOS transistor cell comprising:	'265 Patent: MOS Power Transistor With Improved High-Voltage Capability
	'722 Patent: Method for Making Planar Vertical Cha DMOS Structures
a substrate of semiconductor material of heavily doped first electrical conductivity type;	'265 Patent: Figs. 4-6: N+ layer (10)
	'722 Patent: Figs. 6 and 8: N+ layer (10)
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	'265 Patent: Figs. 4-6: N- layer (12)
a second covering layer of semiconductor material of second electrical conductivity type lying on the first	'722 Patent: Figs. 6 and 8: N- layer (11) '265 Patent: Figs. 4-6: P- layer (20), (21), (22) and (
covering layer;	'722 Patent: Figs. 6 and 8: P layer (20a)
a third covering layer of semiconductor material of heavily doped said first electrical conductivity type and having a top surface and partly lying over the second	'265 Patent: Figs. 4-6: N+ layer (32) and (34) partly lying over P- layer (20) and (22).
covering layer, wherein a portion of the second covering layer is heavily doped and this portion extends both	'265 Patent: Figs. 4-6: a portion of the P- layer is a heavily doped P+ region (21) and (23) and extends be
vertically upward and downward, an upward portion extending through the third covering layer to the top surface of the third covering layer and a downward portion extending downward into the first covering	vertically upward and downward; an upward portion the P+ region extends through the N+ layer (32) and and a downward portion extends downward into the l layer (12).
layer;	'722 Patent: Figs. 6 and 8: N+ layer (21a) partly lyin over P layer (20a)
a trench having a bottom surface and side surfaces and extending vertically downward from the top surface of	'722 Patent: Figs. 6 and 8: groove (31) having a bott surface and side surfaces and extending vertically
the third covering layer through the third covering layer and the second covering layer and through a portion of	downward from the N+ layer (21a) through the N+ la (21a) and the P layer (20a) and through a portion of the N-layer (11)
the first covering layer, wherein the bottom surface of the trench lies above a lowest part of the downward	N- layer (11). '265 patent and '455 patent: the deep P+ region (21)
portion of the second covering layer;	(23) of the '265 patent would be below the lowest po of the grove (42) of the '455 patent
electrically conducting semiconductor material positioned within the trench;	'722.Patent: Figs. 6 and 8: gate (34)
a layer of oxide positioned within the trench between the electrically conducting semiconductor material and the	'722 Patent: Figs. 6 and 8: oxide layer (32) within the groove (31)
bottom and side surfaces of the trench; and three electrically coupled to the electrically	'722 Patent: Fig. 6 and 8: source electrodes (50), dra

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U.S. Patent No. 5		U.S. Patent 4,345,265 In Combination With U.S. Patent 4,767,722
CLAIM 1		
17. A method for providing a trancomprising the steps of:	sistor, said method	'265 Patent: MOS Power Transistor With Improved High-Voltage Capability
		'722 Patent: Method for Making Planar Vertical Char DMOS Structures
providing a first region of a first of	conductivity type;	'265 Patent: Figs. 4-6: N+ layer (10) and N- layer (12
		'722 Patent: Figs. 6 and 8: N+ layer (10) and N- layer (11)
providing a second region of a secover said first region;	cond conductivity type	'265 Patent: Figs. 4-6: P- layer (20), (21), (22) and (2 Col. 3, ln. 42.
		'722 Patent: Figs. 6 and 8: P layer (20a)
providing a third region of said fit such that said first and third region		'265 Patent: Figs. 4-6: N+ layer (32) and (34) partly lying over P- layer (20) and (22).
said second region;		'722 Patent: Figs. 6 and 8: N+ layer (21a)
providing a trench through said the regions; and	nird and second	'722 Patent: Figs. 6 and 8: groove (31) extending vertically downward through the N+ layer (21a) and the P layer (20a)
providing a gate in said trench;		'722 Patent: Figs. 6 and 8: gate (34) in groove (31)
wherein a portion P of said secon- is spaced from said trench, extend trench so that, if a predetermined said gate and to said third region predetermined voltage is applied avalanche breakdown occurs awa said trench.	ds deeper than said voltage is applied to and another to said first region, an	'265 Patent: Col. 5, lns. 32-47 – "The effect of regions and 23 in enhancing the breakdown characteristic of the DMOS structure comes about in several ways. First, the fact that the breakdown occurs at the external peripher of or beneath regions 21 and 22 diverts breakdown from the sensitive channel regions of the DMOS device in the P- regions under the gate 24."
		'265 patent and '722 patent: the deep P+ region (21) a (23) of the '265 patent would be below the lowest poi of the grove (31) of the '722 patent
CLAIM 1	18	or my board (an) or my , and barrens
18. The method of claim 17 wher said second region is doped heav of said second region which portion.	rein said portion P of ier than another portion	'265 Patent: Figs. 4-6: a portion of the P- layer is a heavily doped P+ region (21) and (23) and extends be vertically upward and downward; P+ region (21) and (23) are more heavily doped than P- region (20) and (near the gate region.
AT 1 44 5 1	10	non do gate region.
19. The method of claim 17 when comprises a first portion and a se	rein said first region	'722 patent: Figs. 6and 8: N+ layer (10) under N- layer (11)
first portion, said second portion than said first portion.	-	'265 Patent: Figs. 4-6: N+ layer (10) under N- layer (
CLAIM	20	
20. The method of claim 19 when breakdown is a reach-through breakdown.	rein said avalanche	'265 Patent and '722 Patent: avalanche breakdown would be a reach-through breakdown across the N- la (11) of the '722 Patent

1	CLAIM 22	
	21. The method of claim 17 further comprising the step	'722 Patent: oxide (32)
2	of providing an insulator between said surface of said	
	trench and said gate.	
3	CLAIM 23	
	23. A method for providing a transistor, said method	'265 Patent: MOS Power Transistor With Improved
4	comprising the steps of:	High-Voltage Capability
5		
ر		'722 Patent: Method for Making Planar Vertical Channel
6		DMOS Structures
v	providing a first region of a first conductivity type;	'265 Patent: Figs. 4-6: N+ layer (10)
. 7		(700 P) (710 C) 10 2V 1 (10)
	C 15	'722 Patent: Figs. 6 and 8: N+ layer (10)
8	providing a second region of said first conductivity type	'265 Patent: Figs. 4-6: N- layer (12)
	over said first region, said second region being lighter doped than said first region;	'722 Patent: Figs. 6 and 8: N- layer (11)
9	providing a third region of a second conductivity type	'265 Patent: Figs. 4-6: P- layer (20), (21), (22) and (23)
	over said second region, said second and third regions	over the second region
10	forming a junction;	
.,		'722 Patent: Figs. 6 and 8: P layer (20a)
11	providing a fourth region of said first conductivity type	'265 Patent: Figs. 4-6: N+ layer (32) and (34) partly
12	over said third region;	lying over P- layer (20) and (22).
	,	(722 Patant) Fig. 6 and 9. NJ Javan (21a) northylping
13		'722 Patent: Fig. 6 and 8: N+ layer (21a) partly lying over P layer (20a)
	providing a trench through said fourth region and third	'722 Patent: Figs. 6 and 8: groove (31) through the N+
14	regions; and	layer (21a) and the P layer (20a)
	providing a gate in said trench;	'722 Patent: Figs. 6 and 8: gate (34)
15	wherein a deepest part of said third regions is laterally	'265 Patent: Figs. 4-6: P+ region (21) and (23) is
	spaced from said trench;	laterally spaced from the gate
16	wherein a distance between said deepest part of said	'265 and '722: a distance between said deepest part of a
17	third region and said first region is less than a depletion	third region and a first region would be less than a
1/	width of a planar junction which has the same doping	depletion width of a planar junction which has the same
18	profile as does said junction between said second and	doping profile as does said junction between a second
	third regions at said deepest part of said third region and	and third regions at said deepest part of the third region
19	which is reverse biased around its breakdown voltage.	and which is reverse biased around its breakdown
}	CLAIM 24	voltage.
20	24. The method of claim 23 wherein said deepest part of	'265 Patent: Figs. 4-6: a portion of the P- layer is a
	said third region is doped heavier than a part of said	heavily doped P+ region (21) and (23) and extends both
21	third region which part is adjacent said trench.	vertically upward and downward; P+ region (21) and
		(23) are more heavily doped than P- region (20) and (22)
22	`	near the gate region.
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U.S. Patent 5,072,266	U.S. Patent 4,783,694 In Combination With U.S. Patent 3,412,297
CLAIM 1	
1. A trench DMOS transistor cell comprising:	'694 Patent: Integrated Bipolar-MOS Semiconductor Device with Common Collector and Drain
	'297 Patent: MOS Field-Effect Transistor with a One-
	Micron Vertical Channel
a substrate of semiconductor material of heavily doped first electrical conductivity type;	'694 Patent: Fig. 5: N substrate (40c)
a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	'694 Patent: Fig. 5: N-Epi layer (40)
	'297 Patent: Figs. 4-6: N layer (10)
a second covering layer of semiconductor material of	'694 Patent: Fig. 5: P layer (42), (42a) and (42e)
second electrical conductivity type lying on the first covering layer;	'297 Patent: Figs. 4-6: P layer (12)
a third covering layer of semiconductor material of	'694 Patent: Fig. 5: N+ layer (44) partly lying over P
heavily doped said first electrical conductivity type and	layer (42a) and (42e) where a portion of the P layer (42 is heavily doped P+ and extends vertically upward
having a top surface and partly lying over the second	through the N+ layer (44) and vertically downward into
layer is heavily doped and this portion extends both	the N-Epi layer (40)
vertically upward and downward, an upward portion	
extending through the third covering layer to the top	'297 Patent: Figs. 4-6: N layer (16) partly lying over P
surface of the third covering layer and a downward	layer (12)
portion extending downward into the first covering	·
layer;	
a trench having a bottom surface and side surfaces and	'297 Patent: Figs 4-6: trench (18) extends downward
extending vertically downward from the top surface of	from the top surface of the N layer (16) through the N
the third covering layer through the third covering layer	layer (16), P layer (12) and through a portion of the N
and the second covering layer and through a portion of	layer (10)
the first covering layer, wherein the bottom surface of	
the trench lies above a lowest part of the downward	·
portion of the second covering layer;	
electrically conducting semiconductor material positioned within the trench;	'297 Patent: conductive semiconductor material (24)
a layer of oxide positioned within the trench between the	'297 Patent: oxide (14)
electrically conducting semiconductor material and the	
bottom and side surfaces of the trench; and	
three electrodes electrically coupled to the electrically	'694 Patent: gate (47), source (36) and drain (40c)
conducting semiconductor material, to the third covering layer and to the substrate, respectively.	'297 Patent: electrodes coupled to the gate (24), source
injoi and to the substrate, respectively.	(22) and drain (20)

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1	INVALIDITY CLAIM CHART FOI	R U.S. PATENT NO. 5,298,442
2	U.S. Patent No. 5,298,442	U.S. Patent 4,783,694 In Combination With U.S. Patent 3,412,297
	CLAIM 17	
4	17. A method for providing a transistor, said method comprising the steps of:	'694 Patent: Integrated Bipolar-MOS Semiconductor Device with Common Collector and Drain
6		'297 Patent: MOS Field-Effect Transistor with a One- Micron Vertical Channel
7	providing a first region of a first conductivity type;	'694 Patent: Fig. 5: N-Epi layer (40).
۱ ′		'297 Patent: Figs. 4-6: N layer (10)
8	providing a second region of a second conductivity type over said first region;	'694 Patent: Fig. 5: P layer (42), (42a) and (42e) lying over the N-Epi layer (40)
9.		'297 Patent: Figs. 4-6: P layer (12)
10	providing a third region of said first conductivity type such that said first and third regions are separated by	'694 Patent: Fig. 5: N+ layer (44) partly lying over P layer (42a) and (42e)
11	said second region;	'297 Patent: Figs. 4-6: N layer (16) partly lying over P
12	providing a trench through said third and second	layer (12) '297 Patent: Figs. 4-6: trench (18) through the N layer
13	regions; and providing a gate in said trench;	(16) and the P layer (12) '297 Patent: Figs. 4-6: gate (24) in trench (18)
14	wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said	'694 patent and '297 patent: the deep P+ region (42e) of the '694 patent would be below the lowest point of the
15	trench so that, if a predetermined voltage is applied to	trench (18) of the '297 patent
16	said gate and to said third region and another predetermined voltage is applied to said first region, an	·
17	avalanche breakdown occurs away from a surface of said trench.	
18		
	CLAIM 18	
19	18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion	'694 Patent: Fig. 5: a portion of the P layer is a heavily doped P+ region (42e); the P+ region (42e) is doped
20	of said second region which portion is adjacent said trench.	heavier than the P region (42a) adjacent the gate region.
21	CI AIM 10	
22	19. The method of claim 17 wherein said first region	'694 patent: Fig. 5: N+ layer (40c) under N epi layer (40)
23	comprises a first portion and a second portion over said first portion, said second portion being lighter doped	
24	than said first portion. CLAIM 20	
25	20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said	'694 Patent and '297 Patent: avalanche breakdown would be a reach-through breakdown across the N epi layer
26	second portion. CLAIM 22	1 10/01
20	21. The method of claim 17 further comprising the step	'297 Patent: oxide (14)
27	of providing an insulator between said surface of said trench and said gate.	
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1	CLAIM 23	
	23. A method for providing a transistor, said method	'694 Patent: Integrated Bipolar-MOS Semiconductor
2	comprising the steps of:	Device with Common Collector and Drain
3		'297 Patent: MOS Field-Effect Transistor with a One- Micron Vertical Channel
4	providing a first region of a first conductivity type;	
5	providing a second region of said first conductivity type over said first region, said second region being lighter	'694 Patent: Fig. 2: N-Epi layer (40)
ĺ	doped than said first region;	'297 Patent: Figs. 4-6: N layer (10)
6	providing a third region of a second conductivity type over said second region, said second and third regions	'694 Patent: Fig. 2: P layer (42), (42a) and (42e)
7	forming a junction;	'297 Patent: Figs. 4-6: P layer (12)
8	providing a fourth region of said first conductivity type over said third region;	'694 Patent: Fig. 2: N+ layer (44) partly lying over P layer (42a) and (42e)
9		'297 Patent: Figs. 4-6: N layer (16) partly lying over P layer (12)
10	providing a trench through said fourth region and third regions; and	'297 Patent: Figs. 4-6: trench (18) through N layer (16) and P layer (12)
11	providing a gate in said trench;	'297 Patent: Figs. 4-6: gate (24) in trench (18)
12	wherein a deepest part of said third regions is laterally spaced from said trench;	'694 Patent: Fig. 5: the deepest part of the P region (42e) is laterally spaced form said trench
13	wherein a distance between said deepest part of said third region and said first region is less than a depletion	'694 and '297: a distance between said deepest part of a third region and a first region would be less than a
14	width of a planar junction which has the same doping profile as does said junction between said second and	depletion width of a planar junction which has the same doping profile as does said junction between a second
15	third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.	and third regions at said deepest part of the third region and which is reverse biased around its breakdown voltage.
16	CLAIM 24	Votage
17	24. The method of claim 23 wherein said deepest part of	'694 Patent: Fig. 5: a portion of the P layer is a heavily doped P+ region (42e) and extends both vertically
.,	said third region is doped heavier than a part of said	upward and downward; P+ region (42e) is more heavily
18	third region which part is adjacent said trench.	doped than P region (42a) which is near the gate region.

20	INVALIDITY CLAIM CHART	FOR U.S. PATENT NO. 5,072,266
21	U.S. Patent 5,072,266	U.S. Patent 4,593,302 In Combination With U.S. Patent 3,412,297
22	CLAIM 1	
23	1. A trench DMOS transistor cell comprising:	'302 Patent: Process for Manufacture of High Power MOSFET with Laterally Distributed High Carrier
24		Density Beneath the Gate Oxide
25		'297 Patent: MOS Field-Effect Transistor with a One- Micron Vertical Channel
26	a substrate of semiconductor material of heavily doped first electrical conductivity type;	'302 Patent: Figs. 20 and 22: N+ layer
27	a first covering layer of semiconductor material of said first electrical conductivity type lying on the substrate;	'302 Patent: Figs. 20 and 22: N layer (100)
		'297 Patent: Figs. 4-6: N layer (10)

1	a second covering layer of semiconductor material of	'302 Patent: Figs. 20 and 22: P layer (220) and (221)
	second electrical conductivity type lying on the first	
2	covering layer;	'297 Patent: Figs. 4-6: P layer (12)
	a third covering layer of semiconductor material of	'302 Patent: Figs. 20 and 22: N+ layer (170) and (171)
3	heavily doped said first electrical conductivity type and	partly lying over P layer (220) and (221) where a portion
	having a top surface and partly lying over the second	of the P layer (220) and (221) is heavily doped P+ and
4	covering layer, wherein a portion of the second covering	extends vertically upward through the N+ layer (170) and
	layer is heavily doped and this portion extends both	(171) and vertically downward into the N layer (100)
5	vertically upward and downward, an upward portion	'297 Patent: Figs. 4-6: N layer (16) partly lying over P
	extending through the third covering layer to the top	layer (12)
6	surface of the third covering layer and a downward	\
-	portion extending downward into the first covering	
7	layer;	'297 Patent: Figs 4-6: trench (18) extends downward
8	a trench having a bottom surface and side surfaces and	from the top surface of the N layer (16) through the N
٥	extending vertically downward from the top surface of the third covering layer through the third covering layer	layer (16), P layer (12) and through a portion of the N
9	and the second covering layer and through a portion of	layer (10)
,	the first covering layer, wherein the bottom surface of	
10	the trench lies above a lowest part of the downward	
10	portion of the second covering layer;	
11	electrically conducting semiconductor material	'297 Patent: conductive semiconductor material (24)
	positioned within the trench;	
12	a layer of oxide positioned within the trench between the	'297 Patent: oxide (14)
	electrically conducting semiconductor material and the	
13	bottom and side surfaces of the trench; and	
	three electrodes electrically coupled to the electrically	'320 Patent: gate (132), source (210) and drain (270)
14	conducting semiconductor material, to the third covering	
	layer and to the substrate, respectively.	'297 Patent: electrodes coupled to the gate (24), source
15		(22) and drain (20)

16		
17	INVALIDITY CLAIM CHART FO	R U.S. PATENT NO. 5,298,442
18	U.S. Patent No. 5,298,442	U.S. Patent 4,593,302 In Combination With U.S. Patent 3,412,297
19	CLAIM 17	
20	17. A method for providing a transistor, said method comprising the steps of:	'302 Patent: Process for Manufacture of High Power MOSFET with Laterally Distributed High Carrier Density Beneath the Gate Oxide
21		
22	· -	'297 Patent: MOS Field-Effect Transistor with a One- Micron Vertical Channel
	providing a first region of a first conductivity type;	'302 Patent: Figs. 20 and 22: N+ layer and N layer (100)
23		'297 Patent: Figs. 4-6: N layer (10)
24	providing a second region of a second conductivity type over said first region;	'302 Patent: Figs. 20 and 22: P+ layer (220) and (221) lying over the N layer (100)
25	,	'297 Patent: Figs. 4-6: P layer (12)
26	providing a third region of said first conductivity type such that said first and third regions are separated by	'302 Patent: Figs. 20 and 22: N+ layer (170) and (171) partly lying over P layer (220) and (221)
27	said second region;	'297 Patent: Figs. 4-6: N layer (16) partly lying over P
28		layer (12)

providing a trench through said third and second regions; and	'297 Patent: Figs. 4-6: trench (18) through the N layer (16) and the P layer (12)
 	'297 Patent: Figs. 4-6: gate (24) in trench (18)
wherein a portion P of said second region, which portion	'302 patent and '297 patent: the deep P+ region (220) and (221) of the '302 patent would be below the lowest
trench so that, if a predetermined voltage is applied to	point of the trench (18) of the '297 patent
predetermined voltage is applied to said first region, an	
said trench.	
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CLAIM 18	(200 P F
said second region is doped heavier than another portion	'302 Patent: Figs. 20 and 22: a portion of the P layer is heavily doped P+ region (220) and (221); the P+ region
of said second region which portion is adjacent said trench.	(220) and (221) could be doped heavier than the P region adjacent the gate region.
comprises a first portion and a second portion over said	'302 patent: Figs. 20 and 22: N+ layer under N- layer (100)
than said first portion.	-
breakdown is a reach-through breakdown across said	'302 Patent and '297 Patent: avalanche breakdown would be a reach-through breakdown across the N- layer
	(100)
	/00g D
	'297 Patent: oxide (14)
trench and said gate.	
CLAIM 23	
23. A method for providing a transistor, said method comprising the steps of:	'302 Patent: Process for Manufacture of High Power MOSFET with Laterally Distributed High Carrier
	Density Beneath the Gate Oxide
	'297 Patent: MOS Field-Effect Transistor with a One-
providing a first region of a first conductivity time:	Micron Vertical Channel '302 Patent: Figs. 20 and 22: N+ layer
	'302 Patent: Figs. 20 and 22: N+ layer (100)
over said first region, said second region being lighter	'297 Patent: Figs. 4-6: N layer (10)
providing a third region of a second conductivity type	'302 Patent: Figs. 20 and 22: P layer (220) and (221)
forming a junction;	'297 Patent: Figs. 4-6: P layer (12)
providing a fourth region of said first conductivity type over said third region;	'302 Patent: Figs. 20 and 22: N+ layer (170) and (171) partly lying over P layer (220) and (221)
	'297 Patent: Figs. 4-6: N layer (16) partly lying over P layer (12)
providing a trench through said fourth region and third regions: and	'297 Patent: Figs. 4-6: trench (18) through N layer (16) and P layer (12)
	'297 Patent: Figs. 4-6: gate (24) in trench (18)
DOCSSV2:500277.1	RESPONSE CHART PURSUANT TO CIVIL L.R. 16-9(b) (Case No. C-99-04797 SRA)
	regions; and providing a gate in said trench; wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench. CLAIM 18 18. The method of claim 17 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench. CLAIM 19 19. The method of claim 17 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion. CLAIM 20 20. The method of claim 19 wherein said avalanche breakdown is a reach-through breakdown across said second portion. CLAIM 22 21. The method of claim 17 further comprising the step of providing an insulator between said surface of said trench and said gate. CLAIM 23 23. A method for providing a transistor, said method comprising the steps of: providing a first region of a first conductivity type; providing a second region of said first conductivity type over said first region, said second region being lighter doped than said first region; providing a third region, said second and third regions forming a junction; providing a fourth region of said first conductivity type over said second region of said first conductivity type over said second region of said first conductivity type over said second region, said second and third regions forming a junction; providing a fourth region of said first conductivity type over said third region;

1	wherein a deepest part of said third regions is laterally spaced from said trench;	'302 Patent: Figs 20 and 22: deepest part the third (220) and (221) is laterally spaced from said gate region
2	wherein a distance between said deepest part of said	'302 and '297: a distance between said deepest part of a
	third region and said first region is less than a depletion	third region and a first region would be less than a
3	width of a planar junction which has the same doping	depletion width of a planar junction which has the same
	profile as does said junction between said second and	doping profile as does said junction between a second
4	third regions at said deepest part of said third region and	and third regions at said deepest part of the third region
ı	which is reverse biased around its breakdown voltage.	and which is reverse biased around its breakdown
5		voltage.
1	CLAIM 24	
6	24. The method of claim 23 wherein said deepest part of	'302 Patent: Figs. 20 and 22: a portion of the P layer is a
İ	said third region is doped heavier than a part of said	heavily doped P+ region (220) and (221) and extends
7	third region which part is adjacent said trench.	both vertically upward and downward; P+ region (220)
ļ	_	and (221) could be more heavily doped than P region
8 [-	which is near the gate region.
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Fairchild reserves the right to revise and supplement the claim analysis upon further discovery, investigation and analysis prior to the close of discovery. Additionally, the claim construction found by the Court may significantly alter Fairchild's invalidity arguments.

Fairchild asserts that the '266 and '442 patents are invalid under 35 U.S.C. § 112, ¶ 1, as not containing a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention.

Additionally, Fairchild asserts that claim 1 of the '266 and claims 17, 18, 19, 20, 22, 23 and 24 of the '442 patent are invalid as being indefinite under the 35 U.S.C. § 112, ¶ 2. Claim 1 of the '266 and claims 17, 18, 19, 20, 22, 23 and 24 of the '442 patent fail to distinctly claim the subject matter of the invention. For example, the limitation of claim 23 of the '442 patent "wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage" is indefinite under 35 U.S.C § 112, ¶ 2.

Additionally, Fairchild reserves the right to raise a best mode defense upon completion of discovery, specifically upon completion of the depositions of the inventors

ORRICK HERRINGTON

SUTCLIFFE LLP

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1	In defense of Siliconix's alle	egation of willful infringement, Fairchild intends to rely	
2	upon the opinion(s) of counsel Townsend, Townsend & Crew dated December 23, 1998 and		
3	December 8, 1999. Supplemental invalidit	y/non-infringement opinion(s) will soon be provided to	
4	trial counsel.		
5	Dated: August 30, 2000.	•	
6		TERRENCE P. MCMAHON	
7		WILLIAM L. ANTHONY, JR MONTE COOPER KAI TSENG	
8		THOMAS J. GRAY	
9		ORRICK, HERRINGTON & SUTCLIFFE LLP	
10		Kr. Jane	
11		Kai Tseng Attorneys for Defendant	
12		FAIRCHILD SEMICONDUCTOR, INC.	
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TERRENCE P. McMAHON (State Bar No. 71910) WILLIAM L. ANTHONY, JR. (State Bar No. 106908) MONTE COOPER (State Bar No. 196746) KAI TSENG (State Bar No. 193756) THOMAS J. GRAY (State Bar No. 191411) ORRICK, HERRINGTON & SUTCLIFFE LLP 1020 Marsh Road Menlo Park, CA 94025 Telephone: (650) 614-7400 Facsimile: (650) 614-7401 Attorneys for Defendant,

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

10 SILICONIX INCORPORATED, a 11

Delaware corporation 12

Plaintiff.

FAIRCHILD SEMICONDUCTOR

14

FAIRCHILD SEMICONDUCTOR CORPORATION, a Delaware corporation,

Defendant.

CASE NO: C99-04797 SBA

AMENDED INITIAL DISCLOSURE OF DEFENDANT FAIRCHILD SEMICONDUTOR - PRIOR ART PURSUANT TO CIVIL LOCAL RULE 16-7

AMENDED INITIAL DISCLOSURE OF PRIOR ART PURSUANT I. TO L.R. 16-7(D)

Pursuant to Local Rule 16-7(d), defendant Fairchild Semiconductor Corporation ("Fairchild") makes the following amended initial disclosure of prior art:

Attached hereto is Fairchild's amended initial disclosure of prior art patents, products and publications, and tables categorizing those references. Fairchild's investigation, and its analysis of the listed references, is continuing, and Fairchild reserves the right to supplement and to revise the information provided herein as further analysis is performed, additional information becomes available and discovery is completed. All patents are U.S. patents unless otherwise noted. On information and belief, each listed publication was published at least as early as the date given.

10414-4 JG3

DOCSSV2:503110.1

AMENDED INITIAL DISCLOSURE OF PRIOR ART C 99-04797 SBA

ORRICK, HERRINGTON & SUTCLIFFE LLP

Fairchild incorporates, in full, all references cited (however partially) in the patents-in-suit and/or in their respective file histories, as if fully set forth herein. 2 3 While Fairchild will preliminarily identify pursuant to Local Rule 16-7(e) the prior art references which Fairchild believes anticipates the asserted claims or the combination of 4 prior art references which render the asserted claims obvious, please note that the information in 5 this document is provisional and subject to revision, for the following reasons: 6 7 Fairchild's position on the invalidity of particular claims will depend on (i) how those claims are construed by the Court. Because claim construction has not yet occurred, 8 Fairchild cannot take a final position on the bases for invalidity of disputed claims because the 9 Court may construe those claims to mean something different from what Fairchild presently 10 11 assumes them to mean. 12 Fairchild's search for prior art is on-going. (ii) 13 Fairchild has not completed its discovery from Siliconix Inc. Depositions (iii) of the persons involved in the drafting and prosecution of the patent-in-suit, and of the inventors, 14 15 for instance, will likely reveal information that affects the conclusions herein. 16 PRODUCTION OF DOCUMENTS PURSUANT TO L.R. 16-7(F) II. 17 As required by Local Rule 16-7(f), Fairchild has already produced technical documentation for the Fairchild FDS6680A, the only product accused of infringement in 18 19 Siliconix's Claim Chart. 20 The undersigned certifies that pursuant to local rule 16-6(c) to the best of his knowledge information and belief, formed after a reasonable inquiry, that the disclosure is 21 22 complete and correct, as of this date. 23 Dated: August 30, 2000 24 ORRICK, HERRINGTON & SUTCLIFFE LLP 25 26 27 Attorneys for Defendant 28 Fairchild Semiconductor Corporation ORRICK, HERRINGTON DOCSSV2:503110.1 -2-& SUTCLIFFE LLP 10414-4 103 AMENDED INITIA. SCLOSURE OF PRIOR ART

C 99-04797 5BA

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AMENDED INITIAL DISCLOSURE OF PRIOR ART U.S. Patents No. 5,072,266 & 5,298,422

SILICONIX INC. VS. FAIRCHILD SEMICONDUCTOR CORPORATION

Z	PATENT OR	AUTHOR/	PATENT	ISSUE/
	PUBLICATION TITLE	ASSIGNEE/OR	NUMBER	PUBLICATION
		INVENTOR		DATE
-	Mos Field-Effect Transistor	P.R. Amlinger	U.S. PT. NO.	11/19/68
	With A One-Micron Vertical	•	3,412,297	
	Channel			
2	Integrated Circuit Utilizing	Jean-Claude Frouin et	U.S. PT. NO.	03/10/70
	Dielectric Plus Junction	al.	3,500,139	
	Isolation			
3	Complementary Field-Effect	Roger Cullis	U.S. PT. NO.	06/30/70
	Transistors On Common		3,518,509	
	Substrate By Multiple Epitaxy			
	Techniques			
4	Modified Planar Process For	Loyd H. Clevenger	U.S. PT. NO.	10/13/70
	Making Semiconductor		3,534,234	
	Devices Having Ultrafine		•	
	Mesa Type Geometry	•		
5	Method Of Fabricating	Peltzer	U.S. PT. NO.	03/07/72
	Integrated Circuits, With		3,648,125	
	Integrated Circuits With			
	Oxidized Isolations And The			
	Resulting Structure			

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
6	Method Of Manufacturing	Appels et al.	U.S. PT. NO.	08/19/75	103
	Which Silicon Oxide Regions		3,700,330		
	Inset In Silicon Are Formed				
	By A Masking Oxidation,				
	Wherein An Intermediate				
	Layer Of Polycrystalline				
	Silicon Is Provided Between				
	The Substrate And The				
	Oxidation Mask				
7	Low Capacitance V. Grove	Rodgers	U.S. PT. NO.	12/02/75	102, 103
	Mos Nor Gate And Method		3,924,265		
	Of Manufacture				
œ	Multilevel Conductor	Naber	U.S. PT. NO.	12/09/75	103
	Structure And Method		3,925,572		
y	Semiconductor Device	Webb	U.S. PT. NO.	05/18/76	
	Manufacture		3,958,040		
10	Semiconductor Device	Abbas et al.	U.S. PT. NO.	06/01/76	
	Having Electrically Insulating	-	3,961,355		
	Barriers For Surface Leakage				
	Sensitive Devices And				
	Method Of Forming				
<u>-</u>	Method For Forming	Antipov	U.S. PT. NO.	06/08/76	
	Recessed Dielectric Isolation		3,961,999		
	With A Minimized "Birds				
	Beak" Problem				

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	20	19	18	17	16	15		13	12	NO.
1	Large Value Capacitor	Field Effect Semiconductor Device	Single Igfet Memory Cell With Buried Storage Element	Method For Forming Masks Comprising Silicon Nitride And Novel Mask Structures Produced Thereby	Method Of Manufacturing A Semiconductor Device Utilizing Monocrystalline- Polycrystalline Growth	Method Of Forming Raised Electrical Contacts On A Semiconductor Device	Method For Producing A Semiconductor Device And A Semiconductor Device Produced By Said Method	Dielectrically Isolated Semiconductor Devices	Method For Forming Dielectric Isolation Combining Dielectric Deposition And Thermal Oxidation	PATENT OR PUBLICATION TITLE
	Kendall et al.	Fukuta	Jenne	Magdo et al.	Kaji et al.	Reichert	Kooi	Hochberg	Feng et al.	AUTHOR/ ASSIGNEE/OR INVENTOR
4,017,885	U.S. PT. NO.	U.S. PT. NO. 4,015,278	U.S. PT. NO. 4,003,036	U.S. PT. NO. 4,002,511	U.S. PT. NO. 3,977,378	U.S. PT. NO. 3,993,515	U.S. PT. NO. 3,970,486	U.S. PT. NO. 3,966,577	U.S. PT. NO. 3,966,514	PATENT NUMBER
	04/12/77	03/29/77	01/11/77	01/11/77	12/14/76	11/23/76	07/20/76	06/29/76	06/29/76	ISSUE/ PUBLICATION DATE
,			103							CLASSIFICATION

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
21	Method Of Electrically Isolating Individual Semiconductor Circuits In A Wafer	Nelson et al.	U.S. PT. NO. 4,046,605	09/06/77	
22	Superintegrated V-Grove Isolated Bipolar And Vmos Transistors	Bohn	U.S. PT. NO. 4,048,649	09/13/77	103
23	Fabrication Of Power Field Effect Transistors And The Resulting Structures	Jambotkar	U.S. PT. NO. 4,055,884	11/01/77	
24	Self-Aligned Double Implanted Short Channel V-Grove Mos Device	Ouyang	U.S. PT. NO. 4,065,783	12/27/77	103
25	Vmos Transistor	Wickstrom	U.S. Pt. No. 4,070,690	01/24/78	103
26	Insulated Gate Field Effect Transistor	Ishitani	U.S. PT. NO. 4,072,975	02/07/78	103
27	Field Effect Transistor With A Short Channel Length	Tihani et al.	U.S. PT. NO. 4,101,922	07/18/78	
28	Method For Forming Isolated Regions Of Silicon Utilizing Reactive Ion Etching	Bondur et al.	U.S. PT. NO. 4,104,086	08/01/78	103
29	Epitaxial Method Of Fabricating Single Igfet Memory Cell With Buried Storage Element	Jenne	U.S. PT. NO. 4,105,475	08/08/78	103
30	Semiconductor Memory Device	Masuoka et al.	U.S. PT. NO. 4,115,795	09/19/78	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
31	Method Of Making V-MOS Field Effect Transistor For A	Vinson	U.S. PT. NO. 4,116,720	09/26/78	103
	Dynamic Memory Cell Having Improved Capacitance				
32	Isolation Of Integrated	Murphy et al.	U.S. PT. NO. 4 140.558	02/20/79	103
	Etching And Diffusion		1,110,000		
33	Power Field Effect	Jambotkar	U.S. PT. NO.	03/20/79	
	Transistors		4,145,700		
34	Semiconductor Apparatus	Hendrickson	U.S. PT. NO. 4,148,047	04/03/79	103
35	Method For Fabrication	Anantha et al.	U.S. PT. NO.	07/03/79	
	Vertical NPN And PNP		4,159,915		
	Structures Utilizing Ion-				
	Implantation				
36					103
	High Capacity Dynamic Ram Cell	Tasch, Jr.	U.S. PT. NO. 4.164.751	08/14/79	
37	Method Of Selective	Barlett et al.	U.S. PT. NO.	10/09/79	
	Oxidation In Manufacture Of	•	4,170492	-	
	Semiconductor Devices				
38	VMOS Read Only Memory	Kuo	U.S. PT. NO.	04/15/80	103
39	Semiconductor Memory	Natori et al.	U.S. PT. NO.	04/22/80	
	Device		4,199,772		

Nulliar et al. 0.3. F1. NO. 4,301,324
Harrington et al. U.S. PT. NO
4,262,296
Shealy et al. U.S. PT. NO.
4,225,945
U.S. PT. NO
4,222,792
Lever et al. U.S. PT. NO.
4,222,063
Rodgers U.S. PT. NO.
4,222,062
Trotter et al. U.S. PT. NO
4,219,836
Mcelroy U.S. PT. NO
4,202,916
Chadda U.S. PT. NO.
INVENTOR
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AUTHOR/ PATENT

Z C	PATENT OR	AUTHOR/	PATENT	ISSUE/	CLASSIFICATION
	PUBLICATION TITLE	ASSIGNEE/OR INVENTOR	NUMBER	PUBLICATION DATE	
49	One Device Field Effect	Scheuerlein	U.S. PT. NO.	03/09/82	
	Transistor (FET) AC Stable		4,319,342		
	Random Access Memory				
	(Ram) Array				
50	Method Of Fabricating MOS	Chang et al.	U.S. PT. NO.	04/13/82	
	Field Effect Transistors		4,324,038		
15	Method Of Manufacturing	lwai et al.	U.S. PT. NO.	05/04/82	
	Semiconductor Devices		4,327,476		
52	Insulated Gate Type	Nishizawa	U.S. PT. NO.	06/08/82	
	Semiconductor Device		4,334,235		
53	Combined DMOS And A	Pao et al.	U.S. PT. NO.	08/10/82	
-	Vertical Bipolar Transistor		4,344,081		
	Device And Fabrication				
	Method Therefor				
54	MOS Power Transistor With	Blanchard	U.S. PT. NO.	08/17/82	103
	Improved High-Voltage	-	4,345,265		
	Capability				
55	Silicon Integrated Circuits	Jaccodine et al.	U.S. PT. NO.	10/05/82	
			4,333,080		
56	Power MOSFET With An	Becke et al.	U.S. PT. NO.	12/14/82	103
	Anode Region		4,364,073		
57	V-MOS Device With Self-	Garnache et al.	U.S. PT. NO.	12/14/82	102
	Aligned Multiple Electrodes		4,364,074		
85	Semiconductor Integrated	Crowder et al.	U.S. PT. NO.	12/21/82	103
	Circuit Interconnections		4,364,166		
59	Vertical MOSFET With	Goodman et al.	U.S. PT. NO.	12/28/82	<u>E</u>
	Reduced Turn-On Resistance	-	4,366,495		
60	VMOS Memory Cell And	Hiltpold	U.S. PT. NO.	12/25/83	103
	Method For Making Same		4,369,564		

Method For Manufacturing A Vertical, Grooved MOSFET Power Static Induction Transistor Fabrication High Power MOSFET With Low On-Resistance And High Breakdown Voltage Method Of Fabricating A Semiconductor Device With A Base Region Having A Deep Portion Reactive Sputter Etching Of Polysilicon Utilizing A Chlorine Etch Gas And Process And Process Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Device Planar Structure For High Field Regions Matsumura et al. U.S. PT. NO. 4,376,286 U.S. PT. NO. 4,376,286 U.S. PT. NO. 4,443,931 A,443,931 A,443,931 A,443,931 A,443,931 A,443,931 A,443,931 A,383,885 Chlorine Etch Gas And Process A Semiconductor Device Planar Structure For High Voltage Semiconductor Device Planar Structure For High Voltage Semiconductor Device Matsumura et al. U.S. PT. NO. 4,397,075 A,404,735 A,404,735 A,404,735 A,404,735 A,412,242 U.S. PT. NO. U.S. PT. NO. 4,404,735 A,404,735 A,404,7	NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR	PATENT NUMBER	ISSUE/ PUBLICATION	
Vertical, Grooved MOSFET Power Static Induction Fransistor Fabrication High Power MOSFET With Low On-Resistance And High Breakdown Voltage Method Of Fabricating A Semiconductor Device With A Base Region Having A Deep Portion Reactive Sputter Etching Of Polysilicon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.	61	Method For Manufacturing A	Goodman	U.S. PT. NO.	02/22/83	/83
Power Static Induction Transistor Fabrication High Power MOSFET With Low On-Resistance And High Breakdown Voltage Method Of Fabricating A Semiconductor Device With A Base Region Having A Deep Portion Reactive Sputter Etching Of Polysilicon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.		Vertical, Grooved MOSFET		4,374,455		
High Power MOSFET With Low On-Resistance And High Breakdown Voltage Method Of Fabricating A Semiconductor Device With A Base Region Having A Deep Portion Reactive Sputter Etching Of Polysificon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.	62	Power Static Induction	Cogan	U.S. PT. NO.	03/01/83	1/83
High Power MOSFET With Low On-Resistance And High Breakdown Voltage Method Of Fabricating A Semiconductor Device With A Base Region Having A Deep Portion Reactive Sputter Etching Of Polysiticon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al. Matsumura et al.		Transistor Fabrication		4,3/5,124		
Low On-Resistance And High Breakdown Voltage Method Of Fabricating A Semiconductor Device With A Base Region Having A Deep Portion Reactive Sputter Etching Of Polysilicon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Matsumura et al. Matsumura et al.	63	High Power MOSFET With	Lidow et al.	U.S. PT. NO.	03/0	03/08/83
Breakdown Voltage Method Of Fabricating A Semiconductor Device With A Base Region Having A Deep Portion Reactive Sputter Etching Of Polysilicon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process FET Memory Cell Structure Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al. Matsumura et al.		Low On-Resistance And High		4,376,286		
Method Of Fabricating A Semiconductor Device With A Base Region Having A Deep Portion Reactive Sputter Etching Of Polysilicon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al. Matsumura et al.		Breakdown Voltage			·	
Semiconductor Device With A Base Region Having A Deep Portion Reactive Sputter Etching Of Polysificon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al. Matsumura et al.	64	Method Of Fabricating A	Baliga et al.	U.S. PT. NO.	<u>6</u>	04/24/84
A Base Region Having A Deep Portion Reactive Sputter Etching Of Polysilicon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.		Semiconductor Device With		4,443,931		
Reactive Sputter Etching Of Reactive Sputter Etching Of Polysilicon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al. Matsumura et al.		A Base Region Having A				
Polysilicon Utilizing A Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al. Matsumura et al.	65	Reactive Sputter Etching Of	Mavdan et al	US PT NO	寸	05/17/83
Chlorine Etch Gas FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al. Matsumura et al.		Polysilicon Utilizing A	•	4,383,885		
FET Memory Cell Structure And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al. Matsumura et al.		Chlorine Etch Gas			╁	
And Process Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.	66	FET Memory Cell Structure	Fatula Jr. et al.	U.S. PT. NO.	0	08/09/83
Fabrication Method For High Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.		And Process		4,397,075		
Power MOS Device Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.	67	Fabrication Method For High	Blanchard et al.	U.S. PT. NO.	0	08/16/83
Method For Manufacturing A Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.		Power MOS Device		4,398,339		
Field Isolation Structure For A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.	80	Method For Manufacturing A	Sakurai	U.S. PT. NO.	_	09/20/83
A Semiconductor Device Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.		Field Isolation Structure For		4,404,735		
Planar Structure For High Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.		A Semiconductor Device				
Voltage Semiconductor Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.	69	Planar Structure For High	Herman et al.	U.S. PT. NO.		10/25/83
Devices With Gaps In Glassy Layer Over High Field Regions Semiconductor Device Matsumura et al.		Voltage Semiconductor		4,412,242		
Layer Over High Field Regions Semiconductor Device Matsumura et al.		Devices With Gaps In Glassy				
Regions Semiconductor Device Matsumura et al.		Layer Over High Field				
Semiconductor Device Matsumura et al.		Regions			-	
	70	Semiconductor Device	Matsumura et al.	U.S. PT. NO. 4.412.237		10/25/83

NC.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR	PATENT	ISSUE/	CLASSIFICATION
71	Method Of Fabrication Many	INVENTOR		DATE	
	MOSFET Using Overhang Mask	Kicc	U.S. PT. NO. 4,419,811	12/13/83	
72	Semiconductor Memory Device	Takei	U.S. PT. NO.	02/14/84	103
73	Enhancement Mode IEET	NI: A:	4,432,006		
	Dynamic Memory	NIShizawa	U.S. PT. NO.	02/28/84	
74	Fabrication of MOS	Finle of al	4,404,400		
:	Integrated Circuit Devices		4,450,620	05/29/84	
2	Integrated Circuits	Joy et al.	U.S. PT. NO.	06/19/84	
76	Isolation For High Density Integrated Circuits	Joy et al.	U.S. PT. NO.	06/19/84	
η			1,40,404/		
	Method Of Manufacturing A Self-Aligned U-MOS Semiconductor Device	lwai	U.S. PT. NO. 4,455,740	06/26/84	103
78	Vertical MESFET With	Rice	U.S. PT. NO.	07/10/84	
79	Method For Manufacturing	Cal	4,459,605		
	VLSI Complementary MOS	Schwade et al.	U.S. PT. NO.	07/17/84	103
	Field Effect Transistor	·	4,439,740		
	Circuits In Silicon Gate				-
č	Single Flectroda II MOCEET				
		rio et al.	U.S. PT. NO.	07/24/84	103
<u>«</u>		Temple	U.S. PT. NO.	08/21/84	
	Devices With Integral Shorts		4,466,176		

PUBLICATION TITLE ASSIGNEE/OR NUMBER PUBLICATION INTENT INVENTOR NUMBER PUBLICATION INVENTOR Number Date Date of Action of Fabricating A El-Karach U.S. PT. NO. Bipolar Dynamic Memory Cell V-MOS Filed Effect Pransistor David et al. U.S. PT. NO. Bipolar Dynamic Memory Cell V-MOS Filed Effect Pransistor David et al. U.S. PT. NO. Bipolar Dynamic Memory Cell V-MOS Filed Effect David et al. U.S. PT. NO. Bipolar Dynamic Memory Cell Ulizing Self-Aligned Diffusion and Etching Techniques Method Fabricating Power Method For Fabricating Self-Aligned Diffusion and Etching Techniques Self-Aligned Power MOSFET Love U.S. PT. NO. Beniconductor Devices Self-Aligned Power MOSFET Love U.S. PT. NO. Beniconductor Device With Deep Grip Accessible Via The Surface And Process For Manutacturing Same Method For Forning A Void Beyer et al. U.S. PT. NO. D6/04/85 U.S. PT. NO.	103	07/30/85	U.S. PT. NO.	Ford et al.	Channel Channel	90
NO. PATENT OR AUTHOR NUMBER NUMBER PUBLICATION TITLE INVENTOR NUMBER PUBLICATION					Techniques	
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	having a single-crystal		6,649,625		
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114、	Dram cell and array	Malhi	U.S. PAT NO. 4,651,184	03/17/87	103
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;	integrated circuits having		4,670,768		
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	device with trench		4,672,410		
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		4,717,942		groove surrounding	
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	Stress-Free Isolation Layer				
378	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent:	Sung K. Kwon, Hong S. Yang	U.S. PAT. No. 5,387,539	02/07/95	
	Method of Manufacturing Trench Isolation				
379	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent:	Rashid Bashir, Datong Chen, Francois	U.S. PAT. No. 5,385,861	01/31/95	
	Planarized Trench and Field Oxide and Poly Isolation Scheme				
380	Important Trench Patents (06/11/96) - National Semiconductor - Abstract of Patent:	Cheng H. Huang, Water Lur	U.S. PAT. No. 5,371,036	12/06/95	
	Locos Technology With Narrow Silicon Trench				
381	Important Trench Patents (06/11/96) - National Semiconductor - Abstract of Patent:	Shuichi Harajiri	U.S. PAT. No. 5,348,906	09/20/94	
	Method for Manufacturing Semiconductor Device		·		

Important Trench Patents (00/1796) - National Senuconductor - Abstract of Patent: Isolation Technique for Silicon Germanium Devices; Forming Silicon-Germannium layer on Silicon Subtrate, Etching Trench, Forming Silicon Layer and Dielectric	Trench Isolation for Both Large and Small Areas by Means of Silicon Nodules after Metal Etching; Local Oxidation by Means of Silicon Nodules After Metal Etching of Aluminum-Silicon Alloy is Achieved	Planarization Process for IC Trench Isolation Using Oxidized Polysilicon Filler 383 Important Trench Patents (06/11/96) - National Semiconductor - Abstract of Patent:	NO. PUBLICATION TITLE 382 Important Trench Patents (06/11/96) - National Semiconductor - Abstract of Patent:
uctor - uctor - ue for n Devices; Germannium ubtrate, forming Dielectric	for Both Areas by Nodules ng; Local ans of Wher Metal num-Silicon	Jsing Con Filler ents (06/11/96) uctor	OR N TITLE ents (06/11/96) uctor -
James H. Comfort, David L. Harame, Scott R. Stiffler		Water Lur, Anna Su, Jiunn Y. Wu	AUTHOR/ ASSIGNEE/OR INVENTOR Steven S. Cooperman, Andre I. Nasr
U.S. PAT. No. 5,308,785		U.S. PAT. No. 5,308,786	PATENT NUMBER U.S. PAT. No. 5,346,584
05/03/94		05/03/94	PUBLICATION DATE 09/13/94
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-	PUBLICATION TITLE	ASSIGNEE/OR	NUMBER	PUBLICATION DATE	
385	Important Trench Patents (06/11/96) - National Semiconductor - Abstract of Patent:	Toru Yamazaki	U.S. PAT. No. 5,306,940	04/26/94	
	Semiconductor Device				
	Including a Locos Type Field				
	Oxide Film and a U Trench Penetrating the Locos Film				
386	Important Trench Patents (06/11/96) - National Semiconductor - Abstract of Patent:	Douglas P. Verret	U.S. PAT. No. 5,298,450	03/29/94	
	Process for Simultaneously				
	Fabricating Isolation Structures for Binolar and				
	CMOS Circuits				
387	Important Trench Patents (06/11/96) - National Semiconductor -	Mark S. Rodder	U.S. PAT. No.	06/29/93	
	Abstract of Patent:		0,440,700		
	Trench Isolation Process with				
	Reduced Topography		-		
388	Important Trench Patents (06/11/96)	Stephen J. Gaul,	U.S. PAT. No.	06/08/93	
	- National Senticonductor - Abstract of Patent:	Donnald F.	5,217,919		
		Hemmenway			•
	Method of Forming Island				
	with Polysilicon-Filled				
	Trench Isolation; Forming				
	Silicon Nitride Protective and				
	Polishing Stop Layer,	-			
	Etching, Stripping to Expose				
	Underlays Oxide Layer				

	PUBLICATION TITLE	ASSIGNEE/OR	NUMBER	PUBLICATION DATE
389	Important Trench Patents (06/11/96) National Semiconductor – Abstract of Patent:	Guy R. Freeman	U.S. PAT. No. 5,206,182	04/27/93
	Trench Isolation Process; Prevent Inversion of Sidewall of Trenches			
390	Important Trench Patents (06/11/96) - National Semiconductor - Abstract of Patent:	David Back, Wayne I. Kinney, Jonathan E. Macro, John P. Niemi	U.S. PAT. No. 5,179,038	01/12/93
	High Density Trench Isolation for MOS Circuits			
391	Important Trench Patents (06/11/96) - National Semiconductor - Abstract of Patent:	Mitsuru Sakamott	U.S. PAT. No. 5,168,343	12/01/92
	Semiconductor Integrated			
	Improved Trench Isolation;			
	Surface Grooves of Subtrate			
	are Embedded with Silicon Boron Nitride Dielectric to			
	Isolate Circuit Elements			
392	Important Trench Patents (06/11/96) - National Semiconductor - Abstract of Patent:	Shigeru Morita	U.S. PAT. No. 5,148,258	09/15/92
	Semiconductor Device			
	Having Junction Structure of			
	a Plurality of Elemnt.			
	Isolation Regions			

			Nanba, Takahiro Onai, Takeo Shiba, Katsuyoshi Washio	Semiconductor Device with Optimal Distance Between Emitter and Trench Isolation	
	04/28/92	U.S. PAT. No. 5,109,263	Mastada Horiuchi, Kiyoji Ikeda, Tohru Nakamura, Kazuo Nakazato Mitsuo	Important Trench Patents (06/11/96) - National Semiconductor - Abstract of Patent:	396
				High Performance Vertical Bipolar Transistor Structure Via Self-Aligning Processing Techniques; Semiconductors	
	07/07/92	U.S. PAT. No. 5,128,271	Gary B. Bronner, David L. Harame, Mark E. Jost	Important Trench Patents (06/11/96) – National Semiconductor – Abstract of Patent:	395
				Method for Forming Planarized Shallow Trench Isolation in an Integrated Circuit and a Structure Formed Thereby	
	07/14/92	U.S. PAT: No. 5,130,268	Fusen E. Chen, Fu-Tai Liou	Having Trench Isolation Important Trench Patents (06/11/96) - National Semiconductor - Abstract of Patent:	394
	09/15/92	U.S. PAT. No. 5,148,247	Kazunori Imaoka, Takao Miura	Important Trench Patents (06/11/96) National Semiconductor - Abstract of Patent: Semiconductor Device	393
CLASSIFICATION	ISSUE/ PUBLICATION DATE	PATENT NUMBER	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT OR PUBLICATION TITLE	NO.

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397	Important Trench Patents (06/11/96) - National Semiconductor -	Jestrey E. Brighton, Deems R.	U.S. PAT. No. 5,104,816	04/14/92	
	Abstract of Patent:	Hollingsworth,			
	Polysilicon Self-Aligned	Manuel L. Torreno Jr.,			
	Bipolar Device Including	Douglas P. Verret			
	Trench Isolation and Process				
	of Manufacturing Same;				
	Forming Inlined Isolation				
	Channel in Semiconductor				
398	Important Trench Patents (06/11/96) - National Semiconductor -	Pier L. Crotti, Nadia	U.S. PAT. No.	11/26/91	
	Abstract of Patent:	Iazzi	3,008,202		
	Process for Excavating				
	Trenches with a Rounded		•		
	Bottom in a Silicon Subtrate				
	for Making Trench Isolation				
	Structures				
399	Important Trench Patents (06/11/96) - National Semiconductor -	Clarence W. Teng	U.S. PAT. No.	10/29/91	
	Abstract of Patent:		3,001,033		
	Trench Isolation Process;	•			
	Filling Groove of Silicon		•		
	Semiconductor Subtrate				
	having Insulating Sidewalls				
	and Bottom with Polysilicon,				
	Forming, Then Oxidizing the		•		
	Upper Surface of a		•		
	Polysilicon Layer Which				
	Extends over the Sidewalls			•	

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
400	Important Trench Patents (06/11/96) - National Semiconductor - Abstract of Patent:	Monte A. Douglas	U.S. PAT. No. 5,010,378	04/23/91	
	Tapered Trench Structure and Process				
401	Important Trench Patents (06/11/96) - National Semiconductor - Abstract of Patent:	Michael L. Kerbaugh, Charles W. Koburger III, Brian J.	U.S. PAT No. 5,006,482	04/09/91	
	Forming Wide Dielectric- Filled Planarized Isolation Trenches in Semiconductors; Using Silicon Nitride as Etch Stop	Macheeney			, .
402	Important Trench Patents (06/11/96) - National Semiconductor - Abstract of Patent:	Kunio Aomura	U.S. PAT No. 4,988,639	01/29/91	
·	Method of Manufacturing Semiconductor Devices Using Trench Isolation Method that Forms Highly Flat Buried Insulation Film; Silicon Body with Trenches; Insulation Filling, Masking, Dopes				

			Hiroyuki Nihira	Method of Manufacturing	
	06/05/90	U.S. PAT. No. 4,931,409	Nobuyuki Itoh, Hiroomi Nakajima,	Important Trench Patents (06/11/96) - National Semiconductor - Abstract of Patent	406
				Method of Making a CMOS Device with Trench Isolation Devices	
	12/25/90	U.S. PAT. No. 4,980,306	Masafumi Shimbo	Important Trench Patents (06/11/96) - National Semiconductor - Abstract of Patent:	405
				Trench Isolation Technique to Produce Narrow and Wide Regions	
		·		Method of Fabricating a Semiconductor Device;	
,	12/25/90	U.S. PAT. No. 4,980,311	Isamu Nanios	Important Trench Patents (06/11/96) - National Semiconductor - Abstract of Patent:	404
				Defect Free Trench Isolation Devices and Method of Fabrication; Semiconductors, Insulation, Stress Resistance, Masking, Dielectrics, Field Oxide	
	01/08/91	U.S. PAT. No. 4,983,226	William R. Hunter, Christopher Slawinski, Clarence Teng	Important Trench Patents (06/11/96) - National Semiconductor — Abstract of Patent:	403
CLASSIFICATION	ISSUE/ PUBLICATION DATE	PATENT NUMBER	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT OR PUBLICATION TITLE	NO.

103		Japan 62-16572			414
103	08/15/83	Japan 58-137254			413
·	05/19/88	Japan 63114173 A	lwabuchi Toshiyuki et al.	Semiconductor Device and Manufacture Thereof (Abstract)	412
	02/09/88	Japan 63-031170	Ajika Natsuo	Semiconductor Device and Manufacture Thereof (Abstract)	411
103	08/11/87	U.S. PT. NO. 4,685,196	Lee	Method For Making Planar FET Having Gate, Source And Drain In The Same Place	410
	11/08/94	U.S. PT. NO. 5,362,665	Lu	Method of Making Vertical Dram Cross Point Memory Cell	409
				Method of Forming an Oxide Liner and Active Area Mask for Selective Epitaxial Growth in an Isolation Trench	
	02/13/90	U.S. PAT. No. 4,900,692	F.J. Robinson	Important Trench Patents (06/11/96) - National Semiconductor - Abstract of Patent:	408
				Method of Trench Filling; Integrated Circuit Semiconductor Structure	
	05/08/90	U.S. PAT. No. 4,924,284	Klaus D. Beyer, Victor J. Silvestri	Important Trench Patents (06/11/96) - National Semiconductor - Abstract of Patent:	407
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		INVENTOR		DAIE	
415	Semiconductor Device and Its	Yasuno	JP 56-131960 A	10/15/81	103
	Preparation				
416	Semiconductor Device and	Ucda	JP 57-018365 A	01/30/82	103
	Manufacture Thereof				
417	Insulated Gate Semiconductor	Ashikawa	JP 58-137254 A	08/15/83	102, 103
	Device				
418	High speed high breakdown	Patel	EP 94891 A	11/23/83	103
	voltage Mosfet- has vertical				
	structure with source contact				
	opening extending into gate				
	region				
419	V-Groove Mos Type Field-	Yamamoto	JP 59-080970 A	05/10/84	103
	Effect Transistor				
420	High Withstand Voltage	Tanaka	JP 59-193064 A	11/01/84	103
	Vertical Type Transistor				
	Device				
421	Vertical Type Mosfet	Tominaga	JP 60-028271 A	02/13/85	103
422	Method of Fabricating Power	Vora	US 4,503,598	03/12/85	103
	Mosfet Structure Utilizing				
	Self-Aligned Diffusion and				
	Etching Techniques				
423	Self-Aligned Power Mosfet	Love	US 4, 516, 143	05/07/85	103
	with Integral Source-Base				
	Short and Methods of Making				
424	DMOS transistor - with body	Contiero	EP 179407	04/30/86	103
	channel and source regions		(equivalent to US		
	located in substrate		4,757,032)		
425			JP 61-142775	06/30/86	103

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Manufacture of Vertical Type Semiconductor Device with Groove Section	Sasaki	JP 62-12167 A	01/21/87	102, 103
-0r-				
Method for Manufacturing				
Grooved Vertical				
Semiconductor Device				
Vertical Type Semiconductor	Sasaki	JP 62-016572 A	01/24/87	100 103
Device and Manufacture				102,
DMOS transistor - with	Rlanchard	2000000	01000	
shaped groove providing		(conivalent to US	01110	100
small area electrical contact		4. 682.405)		
Vertical Type Semiconductor	Sasaki	JP 62-046569 A	02/28/87	103
Device and Manufacture	-		!	
11101001				
and Vertical DMOS	Blanchard	US 4, 682, 405	07/28/87 ·	103
Transistors				
Fet for High Reverse Bias	Hendrickson	US 4,735,914	04/05/88	103
Design for Low on Resistance				
Semiconductor Device and	lwabuchi	JP 63-114173 A	05/19/88	102 103
Manufacture Thereof				102, 103
Vertical Mosfet and Method	Morie	US 4.786.953	11/22/88	103
		JP 1-192174	08/02/89	103
		JP 1-310576	12/14/89	103
	PATENT OR PUBLICATION TITLE Manufacture of Vertical Type Semiconductor Device with Groove Section -or- Method for Manufacturing Grooved Vertical Semiconductor Device Vertical Type Semiconductor Device and Manufacture Thereof DMOS transistor – with shaped groove providing small area electrical contact Vertical Type Semiconductor Device and Manufacture Thereof Methods for Forming Lateral and Vertical DMOS Transistors Fet for High Reverse Bias Voltage and Geometrical Design for Low on Resistance Semiconductor Device and Manufacture Thereof Vertical Mosfet and Method of Manufacturing the Same	E Sas h Sas	E ASSIGNEE/OR INVENTOR Sasaki tor Sasaki Blanchard tor Sasaki Hendrickson Wabuchi Morie	AUTHOR/ R ASSIGNEE/OR NUMBER INVENTOR JP 62-12167 A 0 h P 62-12167 A 0 h P 62-12167 A 0 h P 62-016572 A 0 Iter Sasaki JP 62-016572 A 0 Blanchard EP 209949 A (equivalent to US 4, 682, 405) Iter Sasaki JP 62-046569 A 0 Iter Sasaki JP 63-114173 A 0 Iter Morie JP 1-192174 08 JP 1-192174 08 JP 1-192174 08

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436			JP 2-102579	04/16/90	103
437	Insulated gate filed effect transistor	Hideshima et al.	JP 55-146976	11/15/80	102
438	Insulated Gate Semiconductor Device	lto et al.	JP 58-137254	08/15/83	102
439	Vertical-type Semiconductor Device and Manufacturing Method Therefor	Sasaki	JP 62-16572	01/24/87	102
440	Physics and Technology of Power MOSFETs	Sun		02/00/82	102
441	Optimization of Discrete High Power MOS Transistors	Blanchard		12/00/81	102
442	Method for Manufacturing Grooved Vertical Semiconductor Device	Sasaki	JP 62-12167	01/21/87	102
.443	Method for the Formation of Polycrystalline Silicon Layers, and Its Application in the Manufacture of a Self-Aligned, Non Planar, MOS Transistor	Tonnel	U.S. 4,420,379	12/13/83	102
444	Vertical MOSFET	Oshikawa	JP 63-124762	08/15/88	102
445	Conductivity-Modulated MOSFET	lioh et al.	JP 63-224260	09/19/88	102
446	Semiconductor Device	Nakatani	JP 59-181668	10/16/84	102
447	Semiconductor Device	Okabe et al.	JP 54-57871	05/10/79	102
448	High voltage semiconductor switch	Pernyeszi	JP 57-72365	05/06/82	102

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449	High withstand voltage	Tanaka	JP 59-193064	11/01/84	102
	vertical type transistor device		10.00.000	020206	
450	Venical MOSFET	Lommaga	JP 60-282/1	02/13/85	102
451	Semiconductor Device and Its Method of Manufacture	Ueda et al.	JP 57-18365	01/30/82	102
452	V-groove MOS Field Effect Transistor	Yamamoto	JP 59-80970	05/10/84	102
453	MOS Power Transistor with Improved High-Voltage Capability	Blanchard	U.S. 4,345,265	08/17/82	103
454	Method of Fabricating a Semiconductor Device with a Base Region Having a Deep Portion	Baliga et al.	U.S. 4,443,931	04/24/84	103
455	MOSFET with Perimeter Channel	Ford et al.	U.S. 4,532,534	07/30/85	103
456	Method for Manufacturing a Vertical, Grooved MOSFET	Goodman	U.S. 4,374,455	02/22/83	103
457	MOS-Field Effect Transistor with a One-Micron Vertical Channel	Amlinger	U.S. 3,412,297	11/19/68	103
458	Integrated Bipolar-MOS Semiconductor Device with Common Collector and Drain	Merrill et al.	U.S. 4,783,694	11/08/88	103

NO.	PATENT OR PUBLICATION TITLE	AUTHOR/ ASSIGNEE/OR INVENTOR	PATENT NUMBER	ISSUE/ PUBLICATION DATE	CLASSIFICATION
459	Process for Manufacture of High Power MOSFET with Laterally Distributed High Carrier Density Beneath the Gate Oxide	Lidow et al.	U.S. 4,593,302	06/03/86	103
460	Design of New Structural High Breakdown Voltage V- MOSFET	Katoh et al.		1983	102
461	A Study for High Voltage V- MOS Structure [Japanese]	Kato et al.		1981	102
462	Design of High Breakdown Voltage V-MOSFET Applying Static Shield Effect	Kato et al.		1983	102
463	High Voltage-ization Using Static Shield Effect	Kato et al.		1984	102
464	U-MOS Power MOSFET	Ueda et al.		04/00/83	102
465	Method for the Formation of Polycrystalline Silicon Layers, and its Application in the Manufacture of a Selfaligned, non planar, MOS Transistor	Tonnel	U.S. 4,420,379		·
466	Integrated Circuit and Method of Fabrication	Wakefield et al.	U.S. 3,793,721	02/26/74	·
467	Gas-Etching Device	Horiike	U.S. 4,192,706	03/11/80	
468	Semiconductor Device with Isolation Between MOSFET and Control Circuit	Takagi et al.	U.S. 4,879,584	11/07/89	

- 4×	480	479	C	C	<u>و</u>	1	478 In	477 SI	476 H	475 L:	474 Bi	473 Bi	472 To St	471 Lo	470 Pc Sc Tr	469 M In Ti	NO.
			Characteristics	Controlled Avalanche	Gate Structure with	Transistors Having Closed	Integrated Gate Field Effect	Split Row Power JFET	High Density, High Voltage Power FET	Lateral Bidirectional Shielded Notch FET	Bidirectional Power FET with Field Shaping	Bidirectional Power FET with Integral Avalanche Protection	Termination of the Power Stage of a Monolithic Semiconductor Device	Low On-Resistance Power MOS Technology	Power Metal-Oxide- Semiconductor Field Effect Transistor	Method of Manufacturing an Insulated Gate Field Effect Transistor	PATENT OR PUBLICATION TITLE
j							Dingwall	Benjamin et al.	Benjamin et al.	Schutten et al.	Schutten et al.	Schutten et al.	Zambrano et al.	Yilmaz et al.	Yilmaz	Ueno	AUTHOR/ ASSIGNEE/OR INVENTOR
Taiwan 762/3	Taiwan 84398	Taiwan 79217	-				U.S. 4,173,022	U.S. 4,635,084	U.S. 4,571,606	U.S. 4,571,512	U.S. 4,553,151	U.S. 4,577,208	U.S. 5,317,182	U.S. 5,304,831	U.S. 5,168,331	U.S. 5,086,007	PATENT NUMBER
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	-		-	MOSFET with an Ron Area	
	12/07/86		Ueda et al.	Deep-Trench Power	509
				Characteristics, IEDM 86	
				Quasi-Saturation	
	-			Improved On-Resistance and	
	1986		Darwish	VDMOS Transistors with	508
				Devices	
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				Characteristics in Trench	•
	09/00/91		Mizuno et al.	High Performance	507
				Conference 1982	
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				MOSFETS, IEEE Power	
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ľ				Specialists Conference 1985	
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				to Add an Overvoltage Self-	
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515	A Low-voltage Power	Rittenhouse and		1990	
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517	Higher power ratings extend V-MOS FETs' dominion, Electronics
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519	Geometry Effects in VMOS Transistors, IEDM 1978
520	Minimization of Parasitic Capacitances in VMOS Transistors, <i>Technical Digest</i>
521	V-Groove Power Field Effect Transistors, <i>Technical Digest</i> 1977, IEDM
522	A Fully Implanted V-Groove Power MOSFET, IEDM 1978
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	18th Conference on Solid State Devices and Materials

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